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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK
APPD

DATE

2010-08-05

SCHEM, FLYING_CLOUD, MLB, K90i

"EVT3"11/22/10

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051-8658	1	SCHEM, MLB, K90i	SCH	CRITICAL	
820-2936	1	PCBF, MLB, K90i	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Mon Nov 22 19:21:11 2010

SCHEM, FLYING_CLOUD, MLB, K90i

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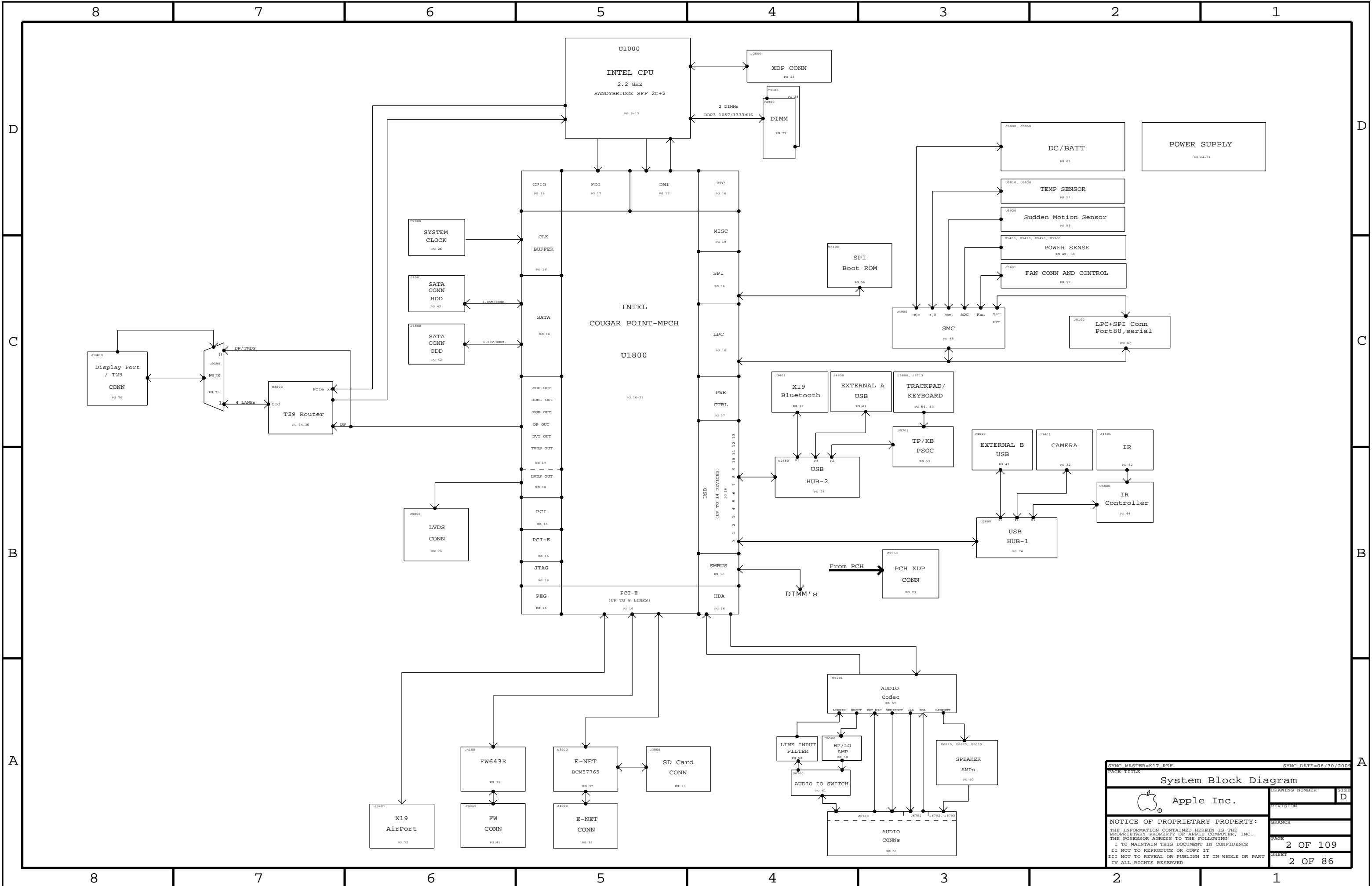
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System Block Diagram

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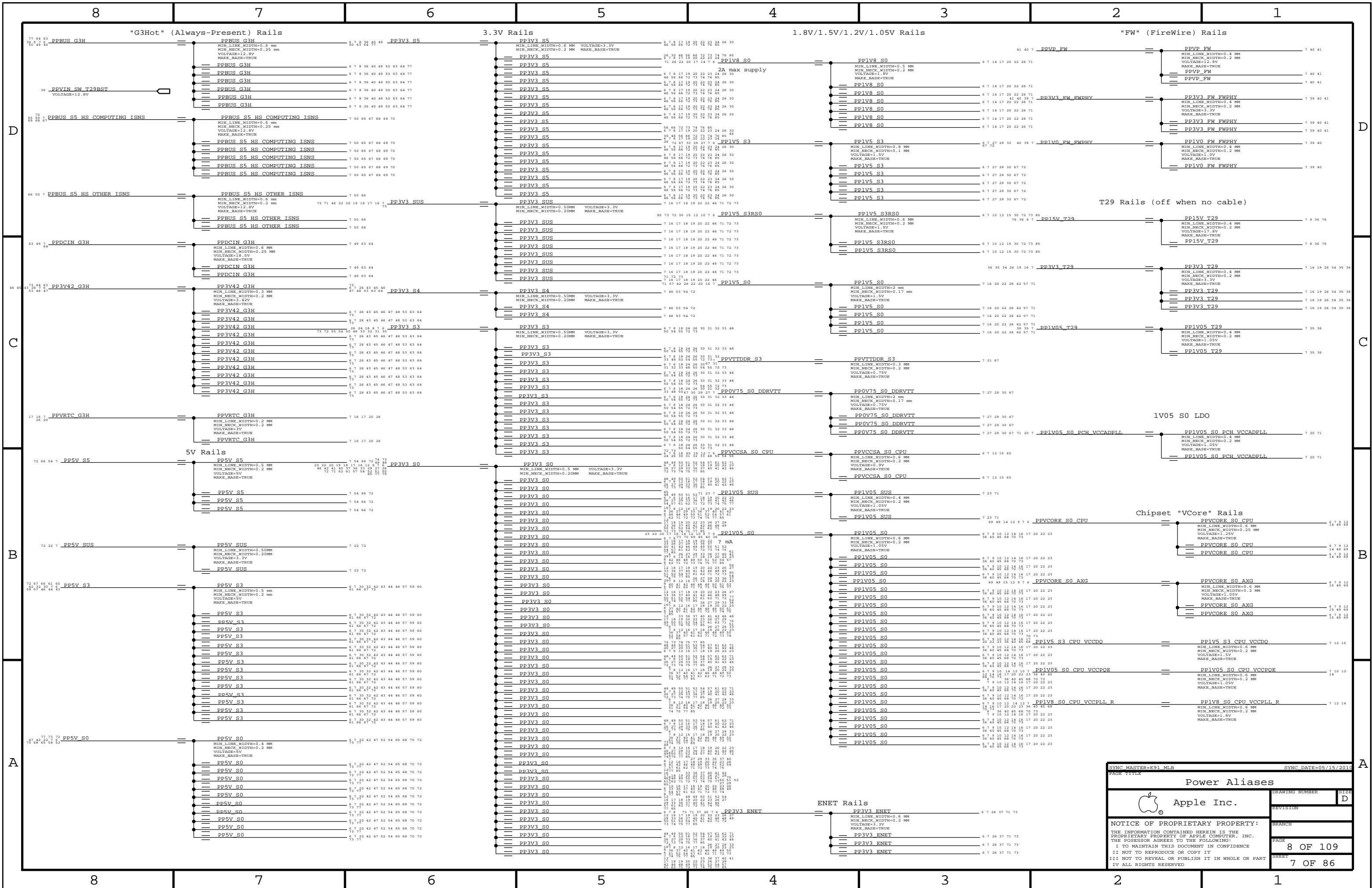
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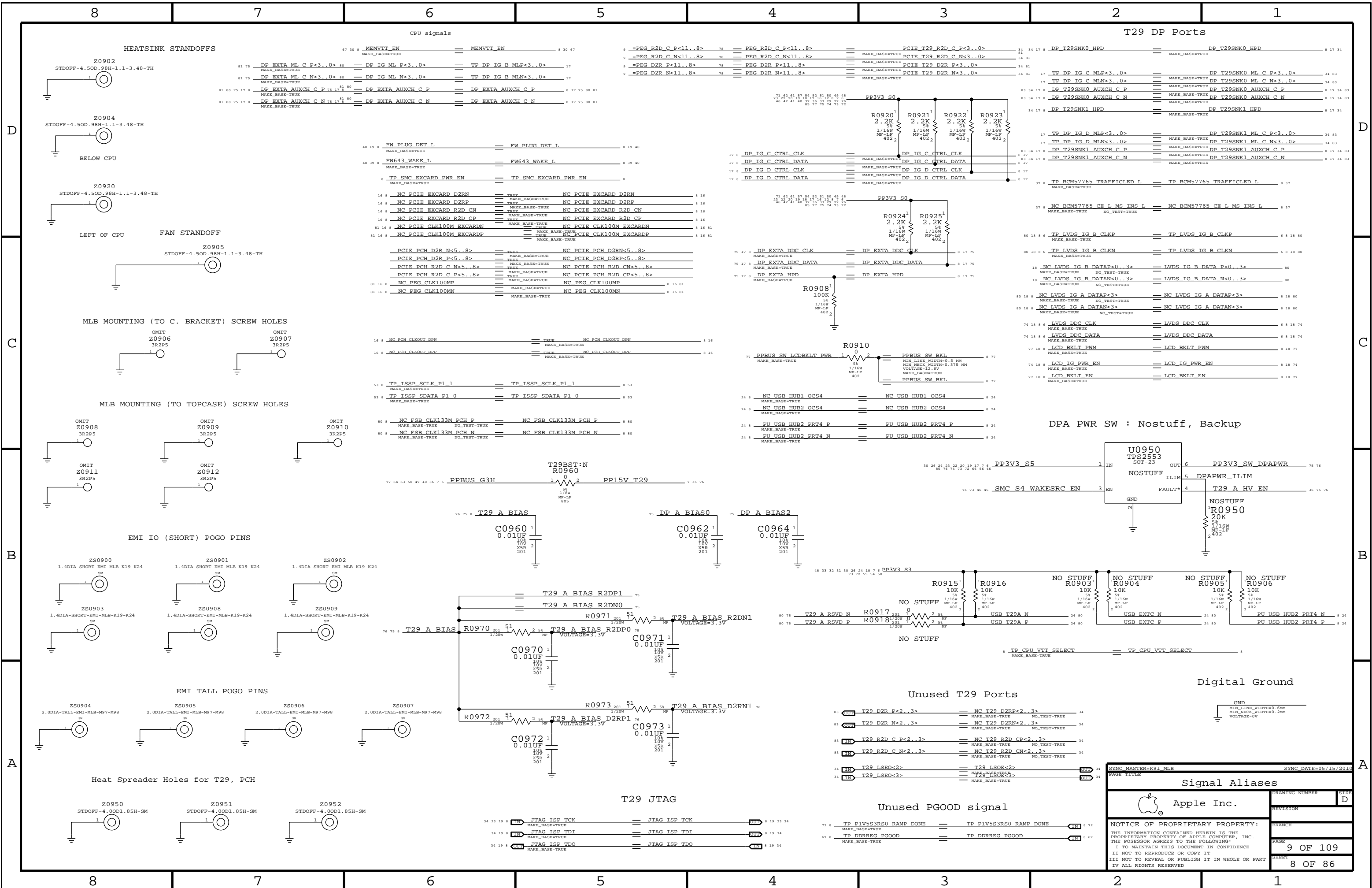
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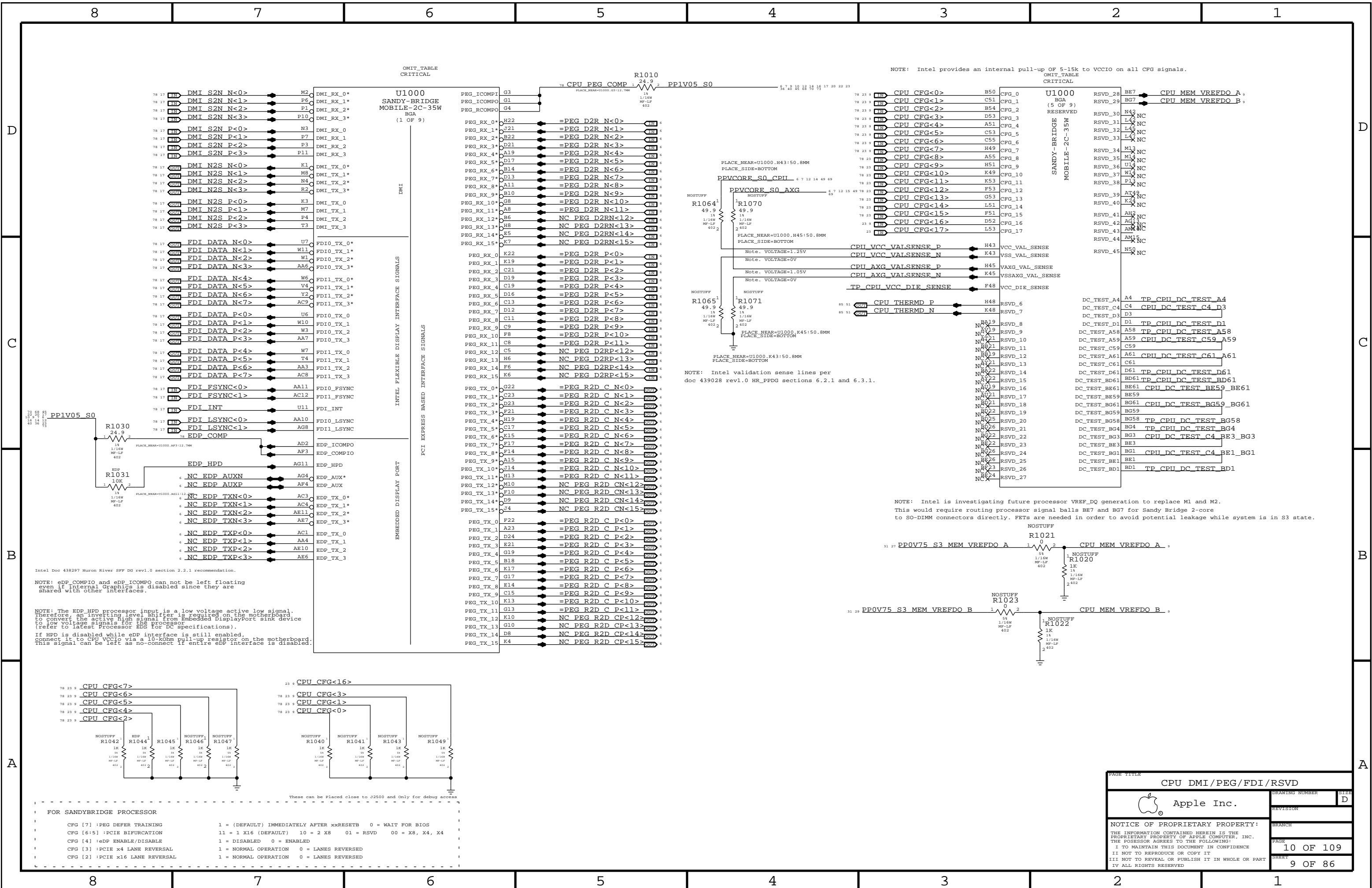
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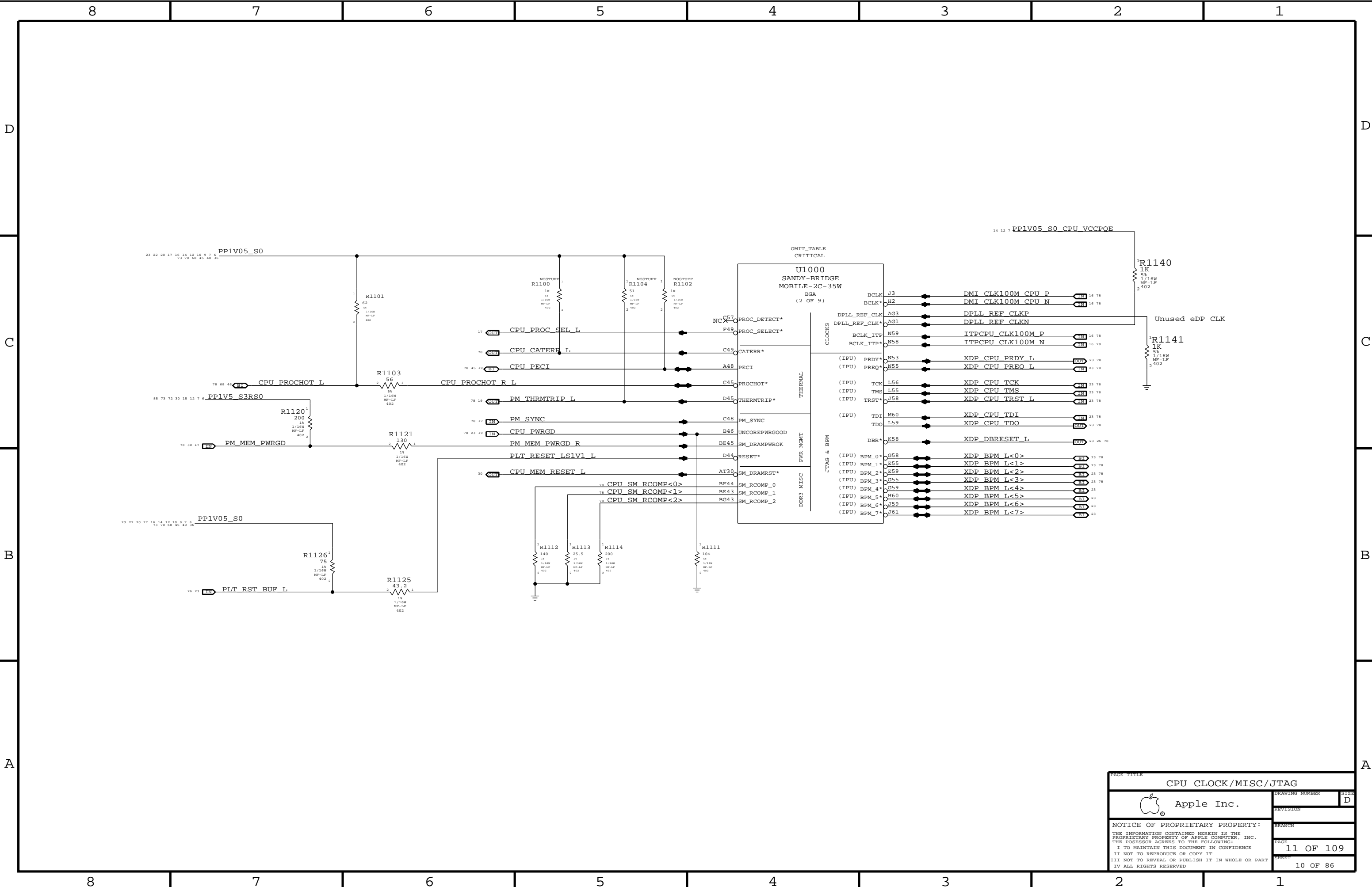
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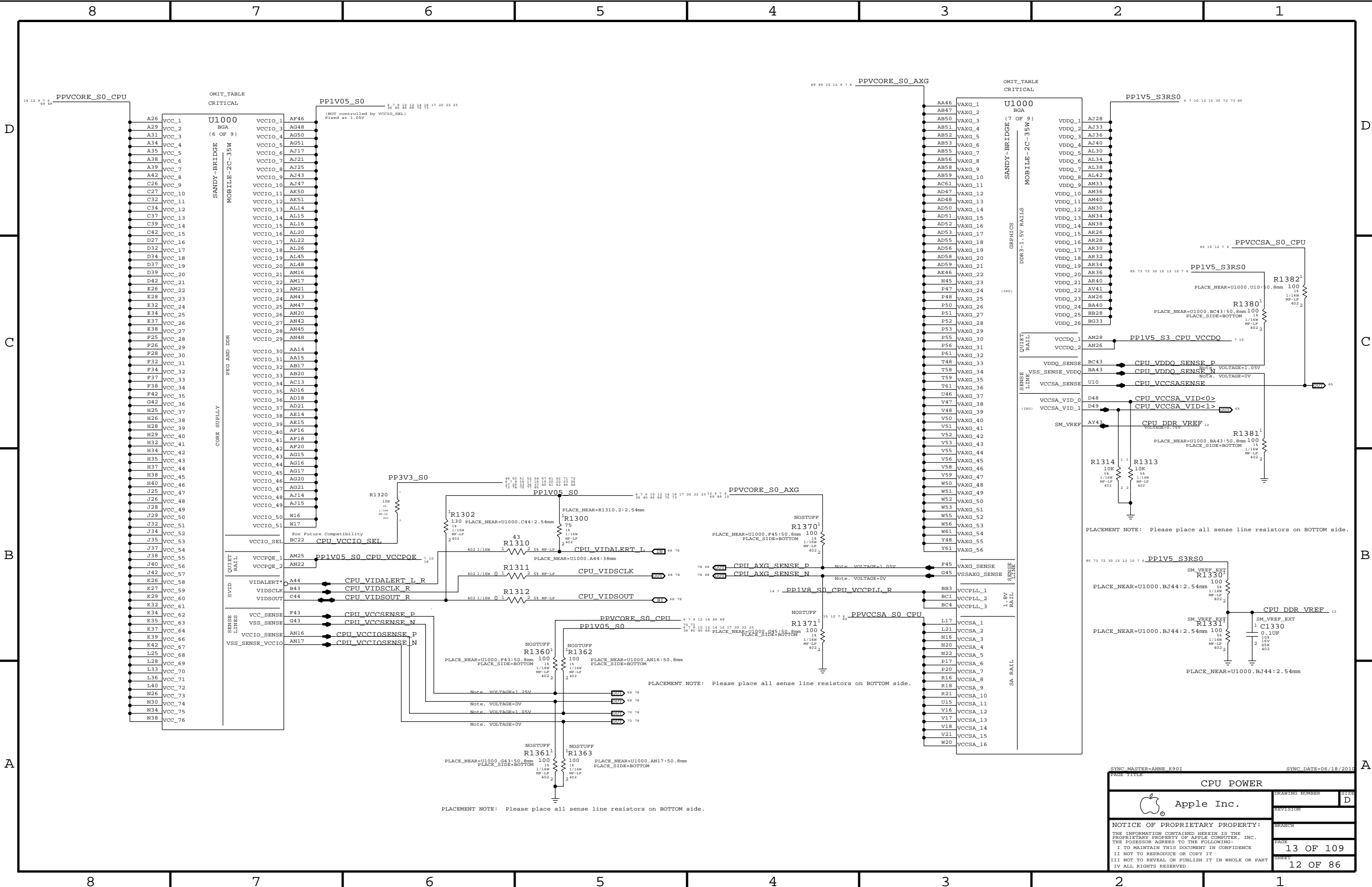




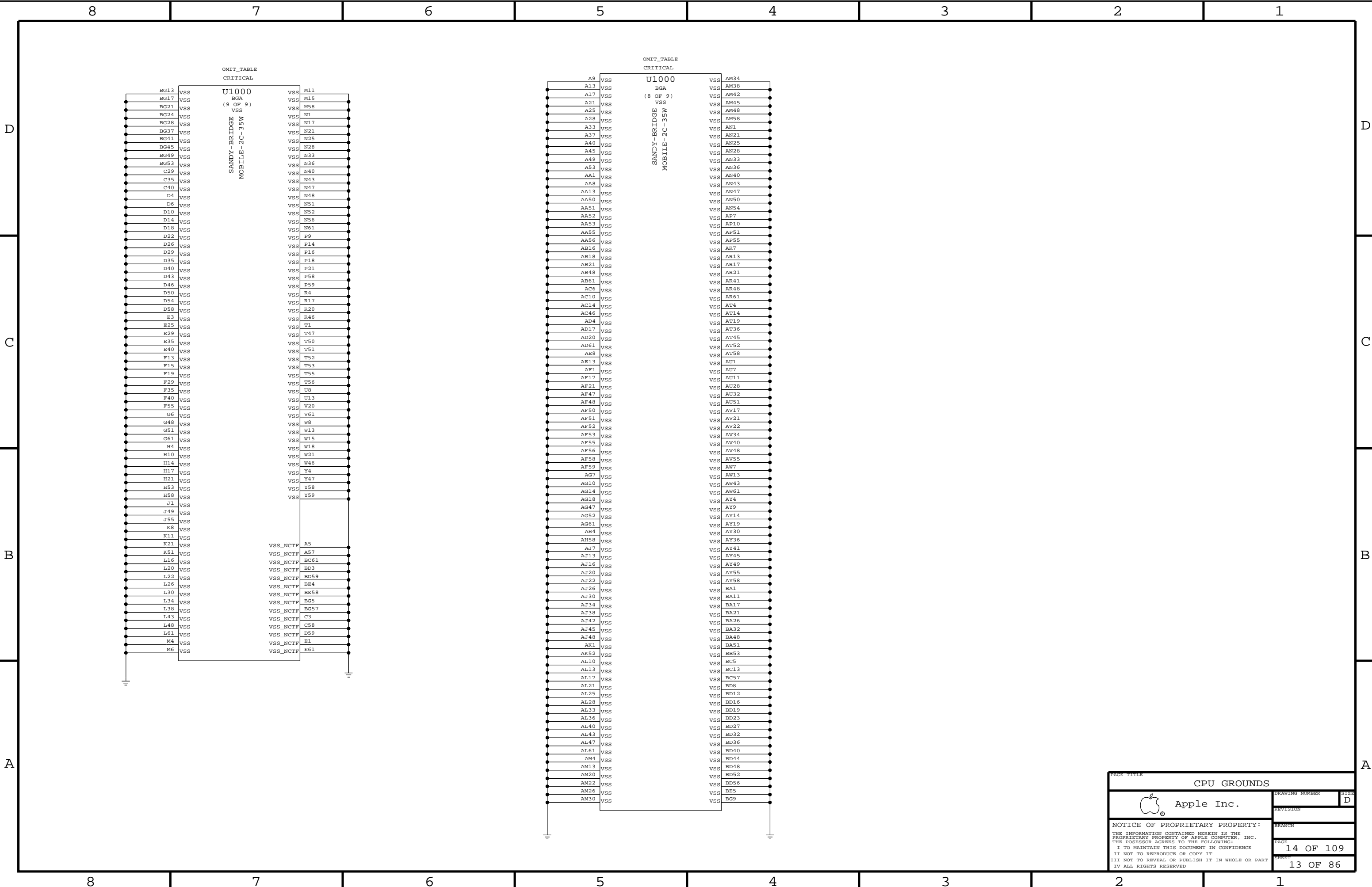


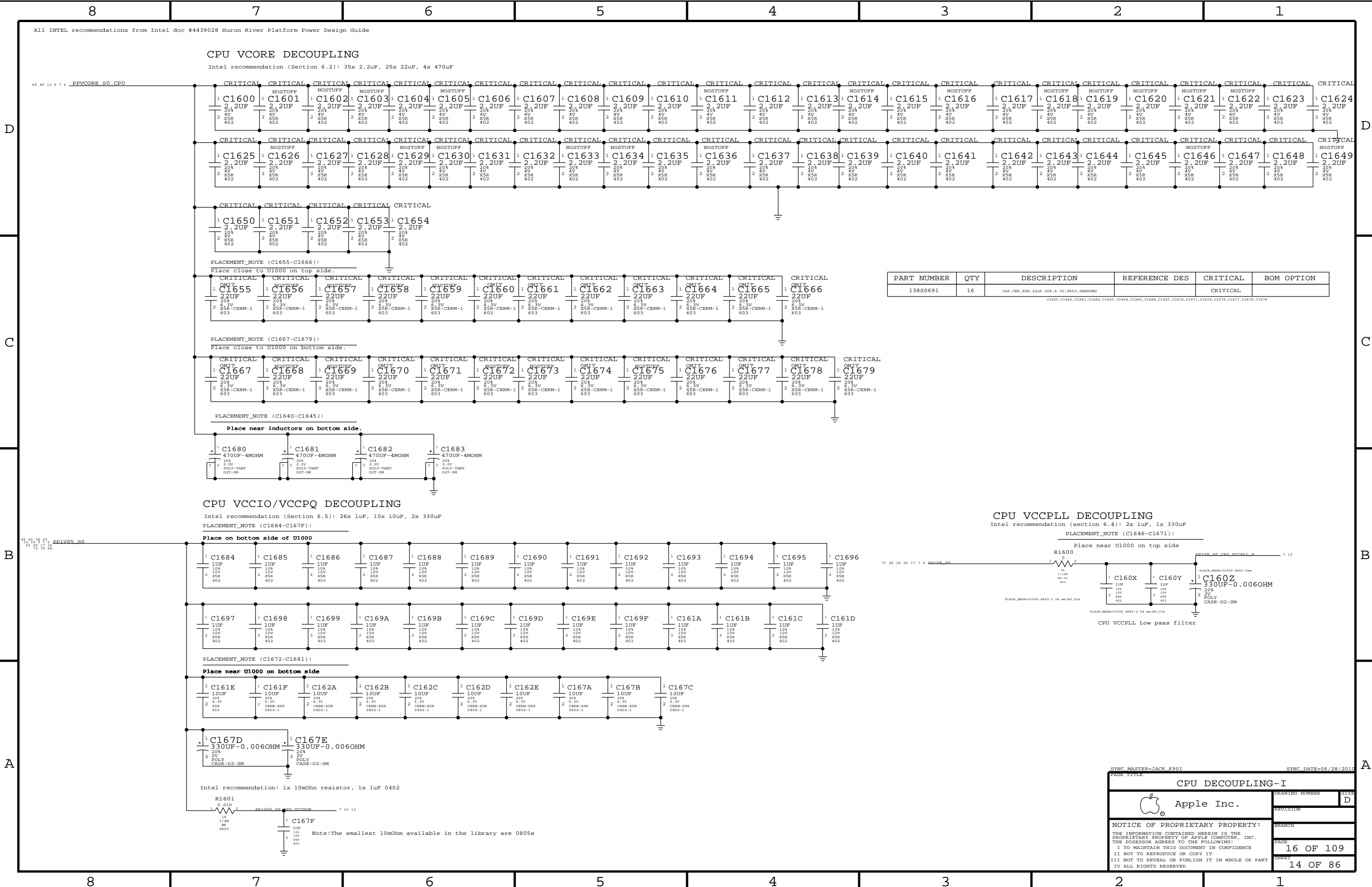






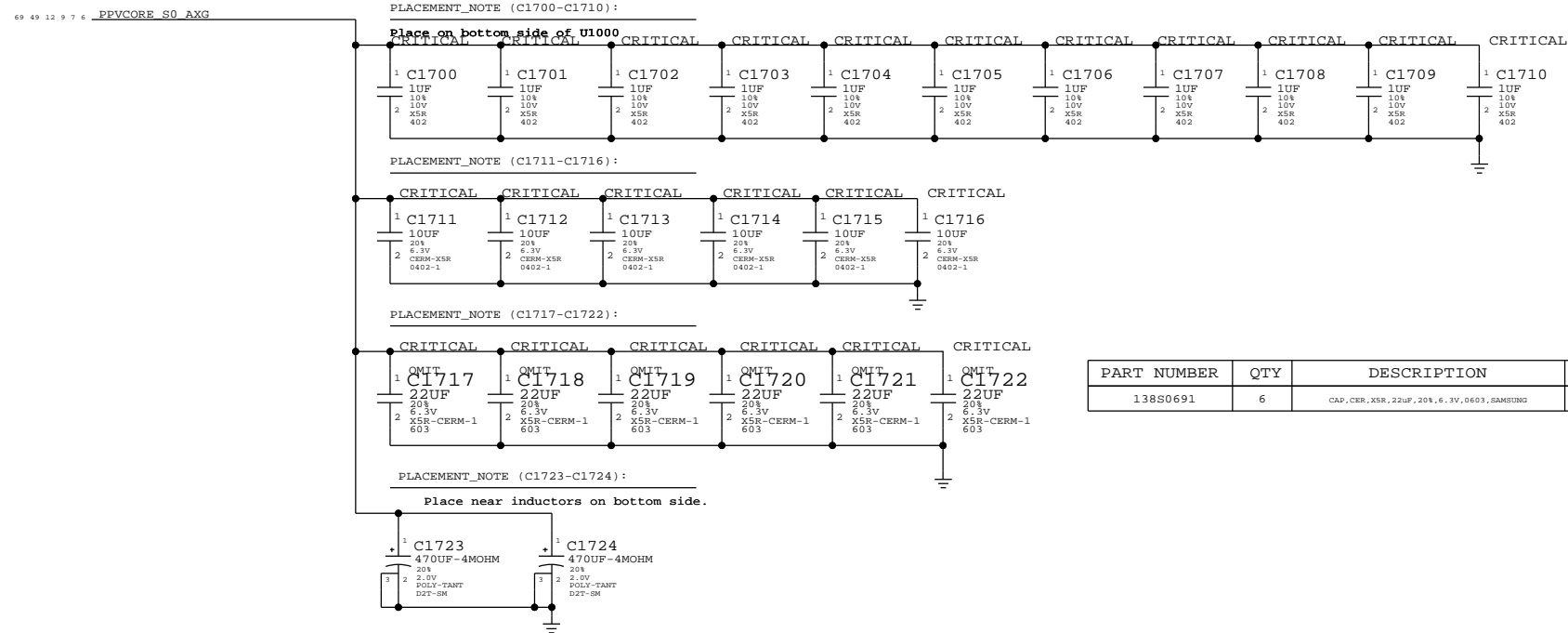
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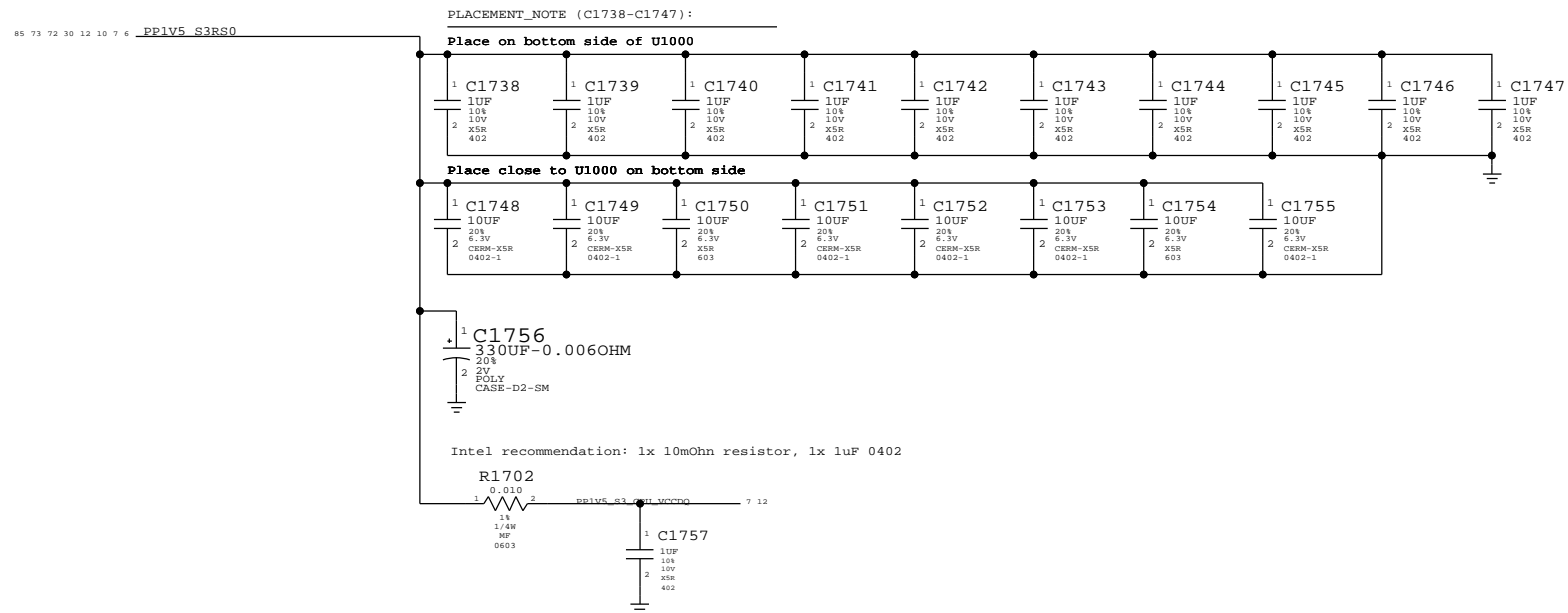
Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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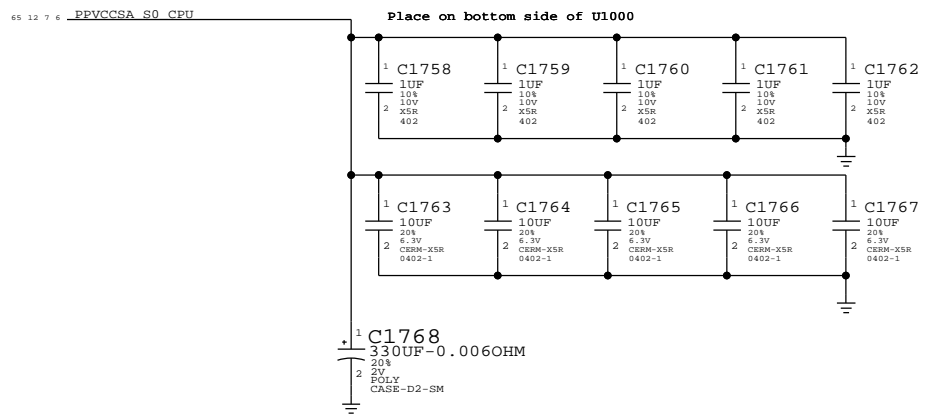
CPU VDDQ/VCCDQ DECOUPLING

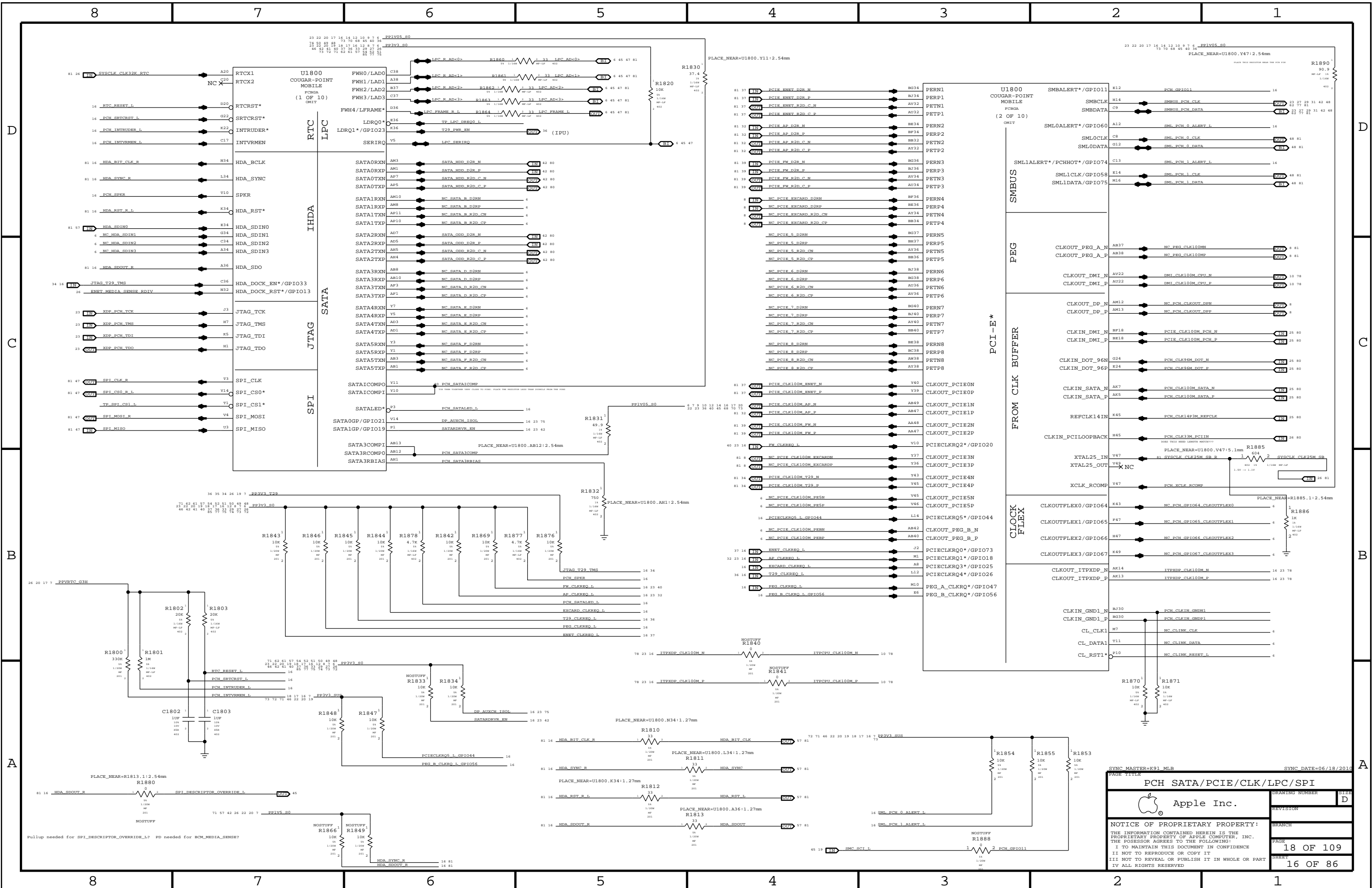
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

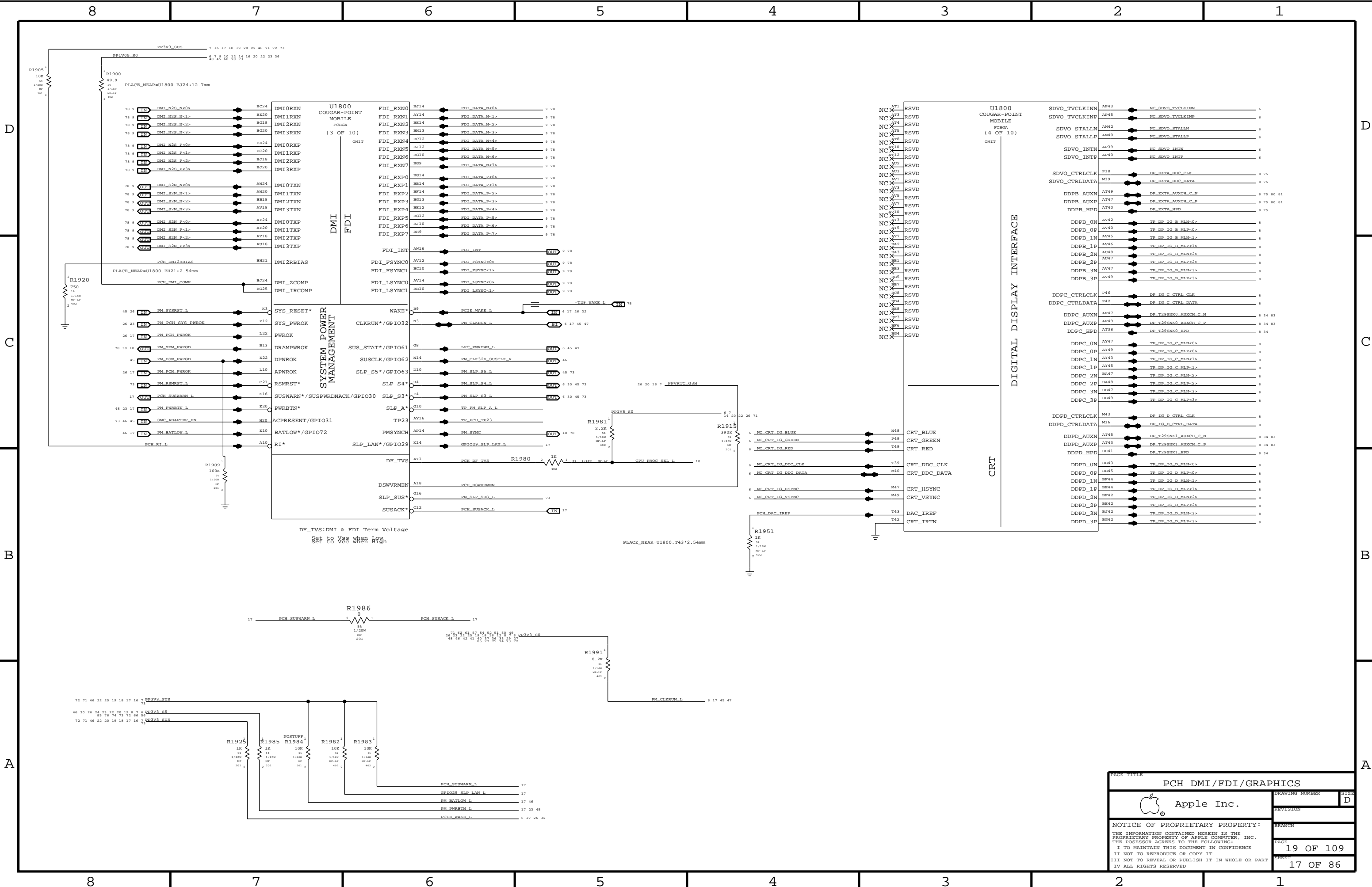


CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uF, 5x 10uF, 1x 330uF

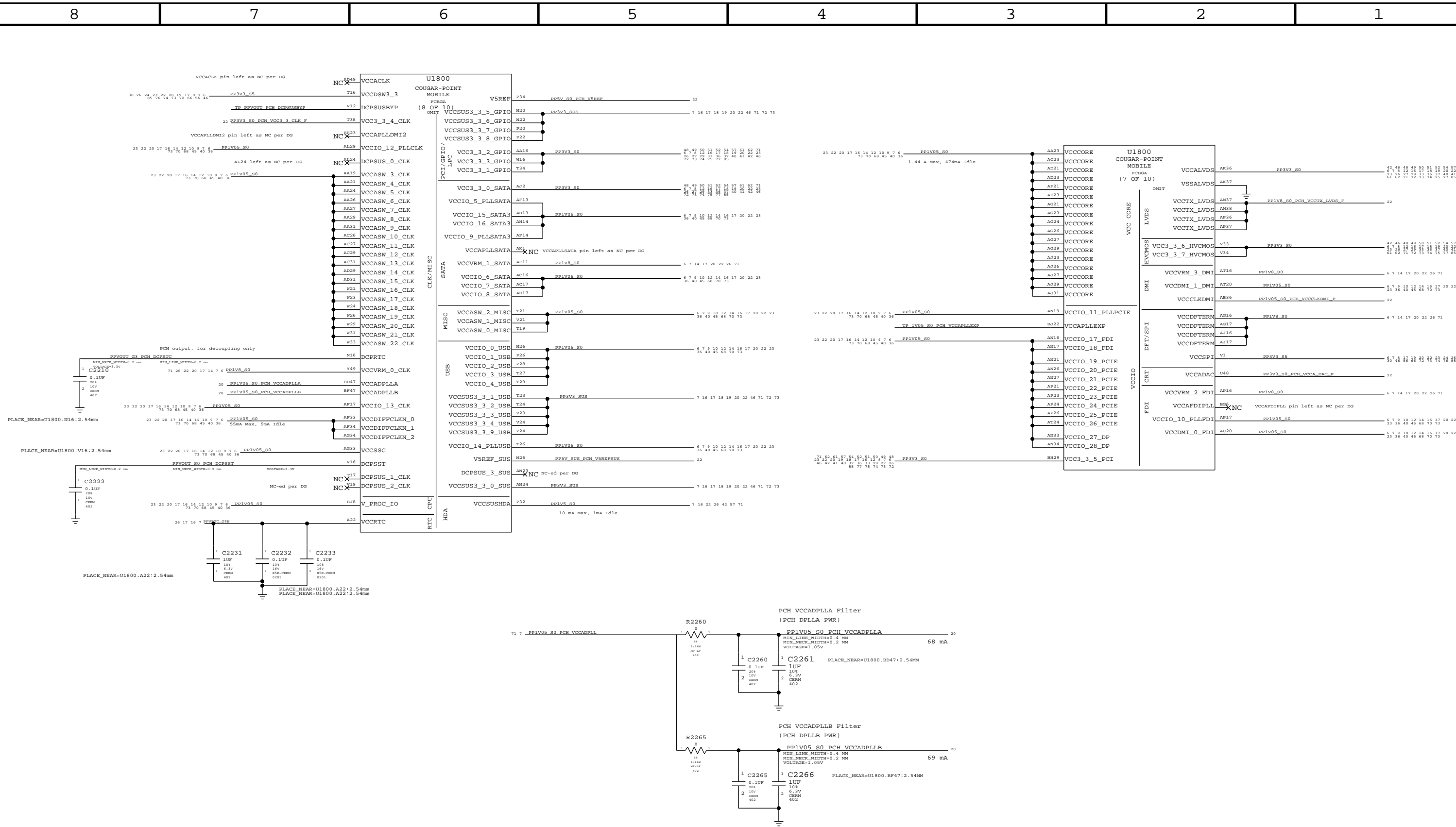













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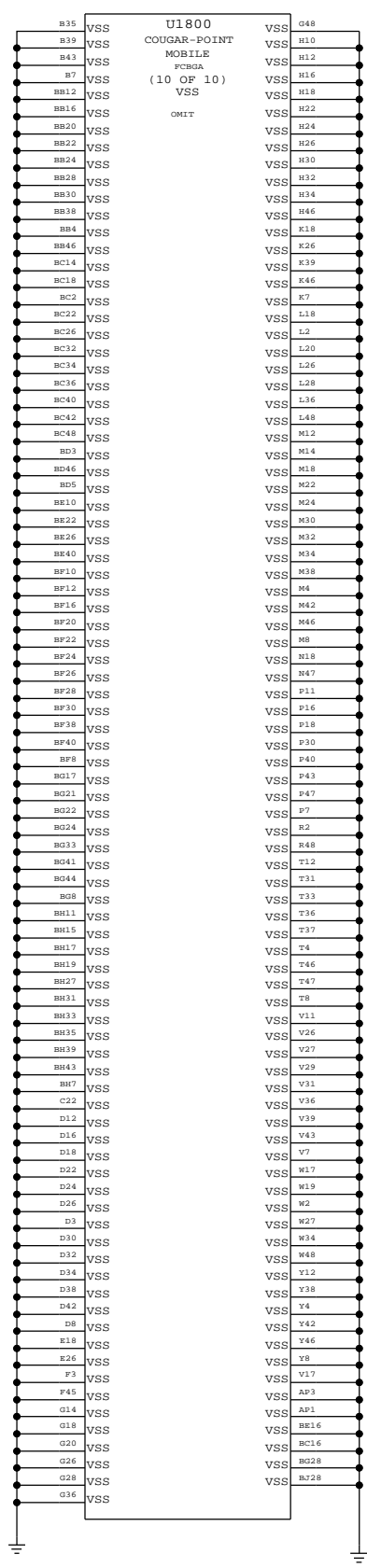
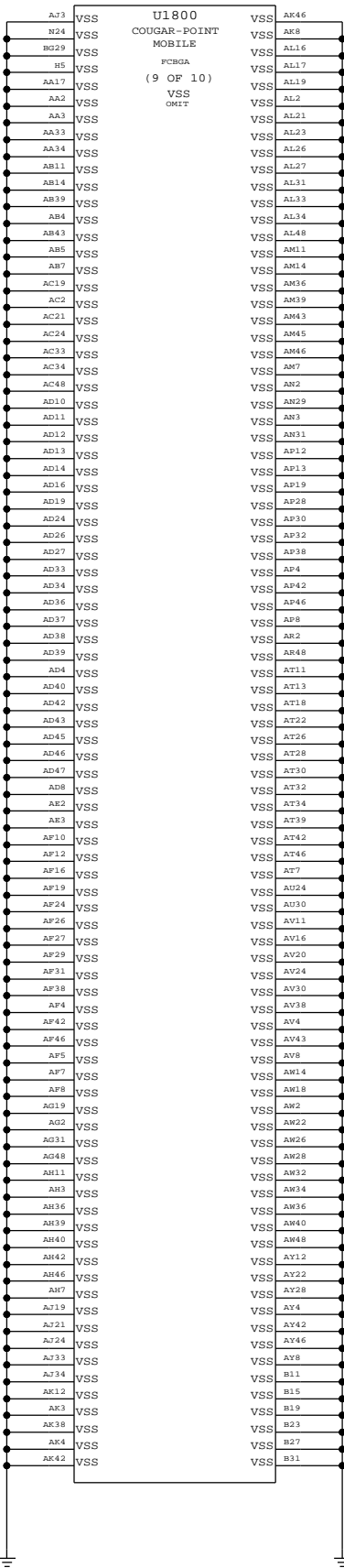
A

D

C


B

A

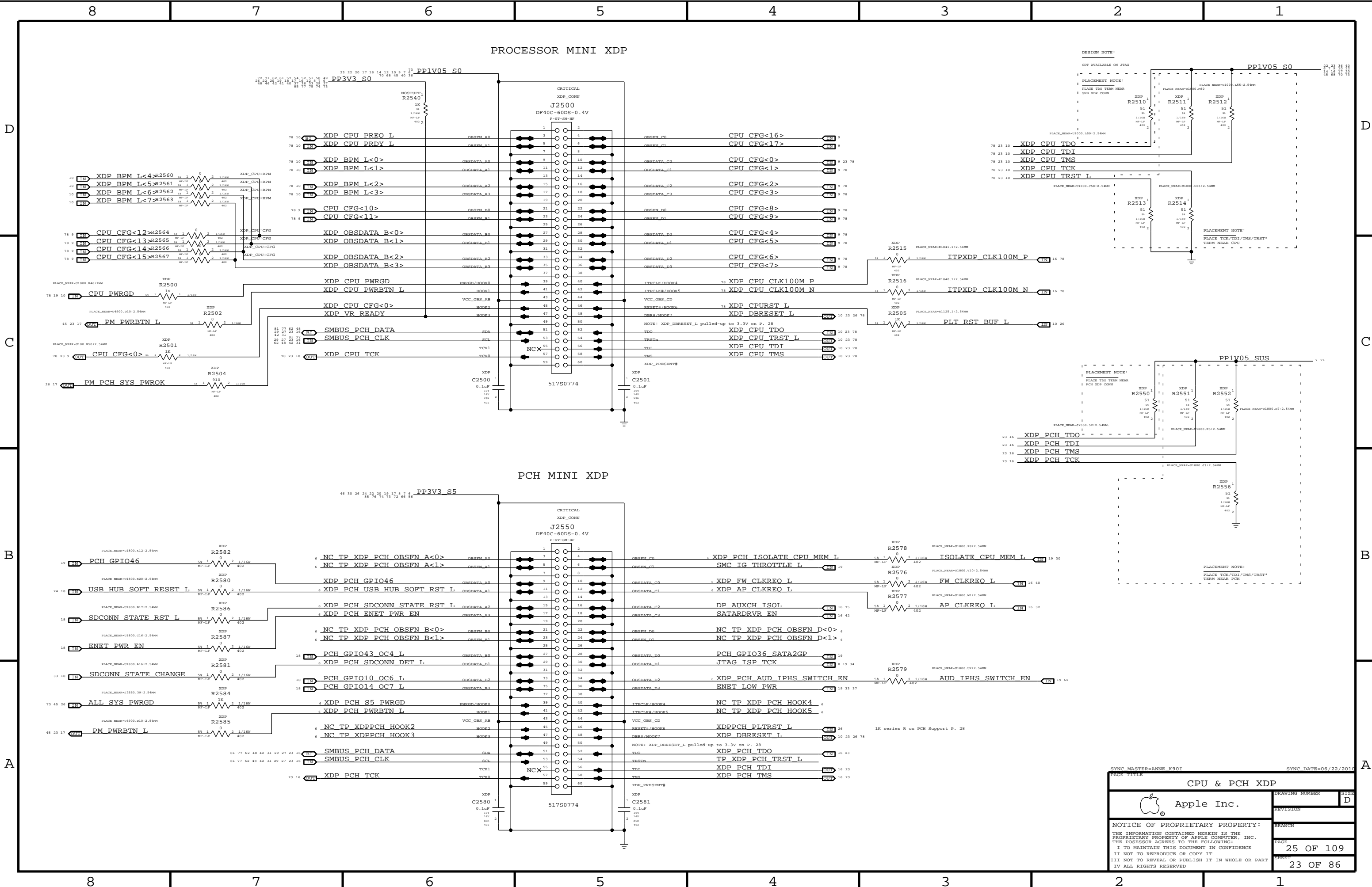


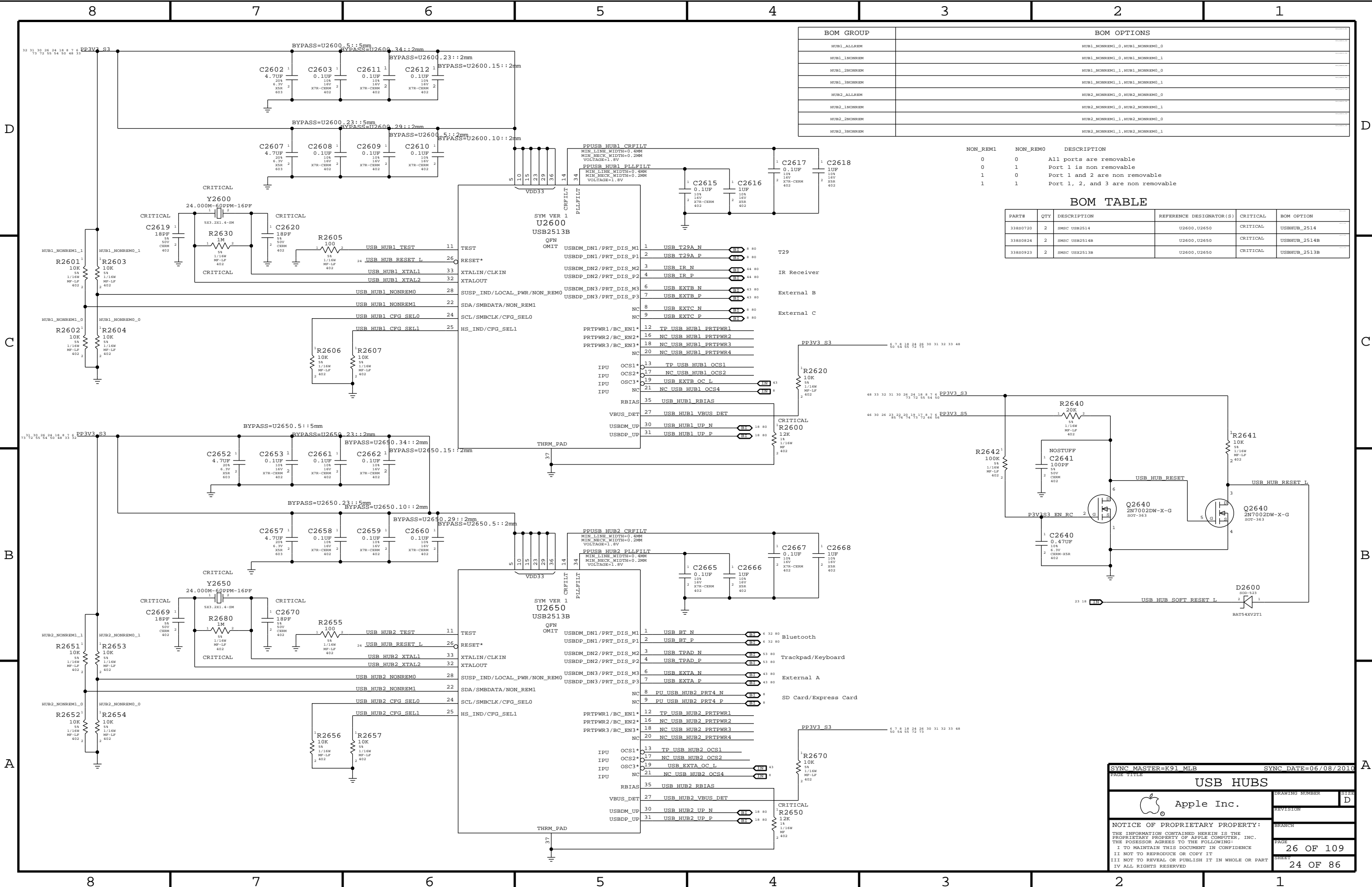
SYNC MASTER=K91 MLB

SYNC DATE=05/27/2010

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		PAGE	23 OF 109
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33850720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
33850824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
33850923	2	SMSC USB2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC MASTER=K91 MLB

SYNC DATE=06/08/2010

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Apple logo

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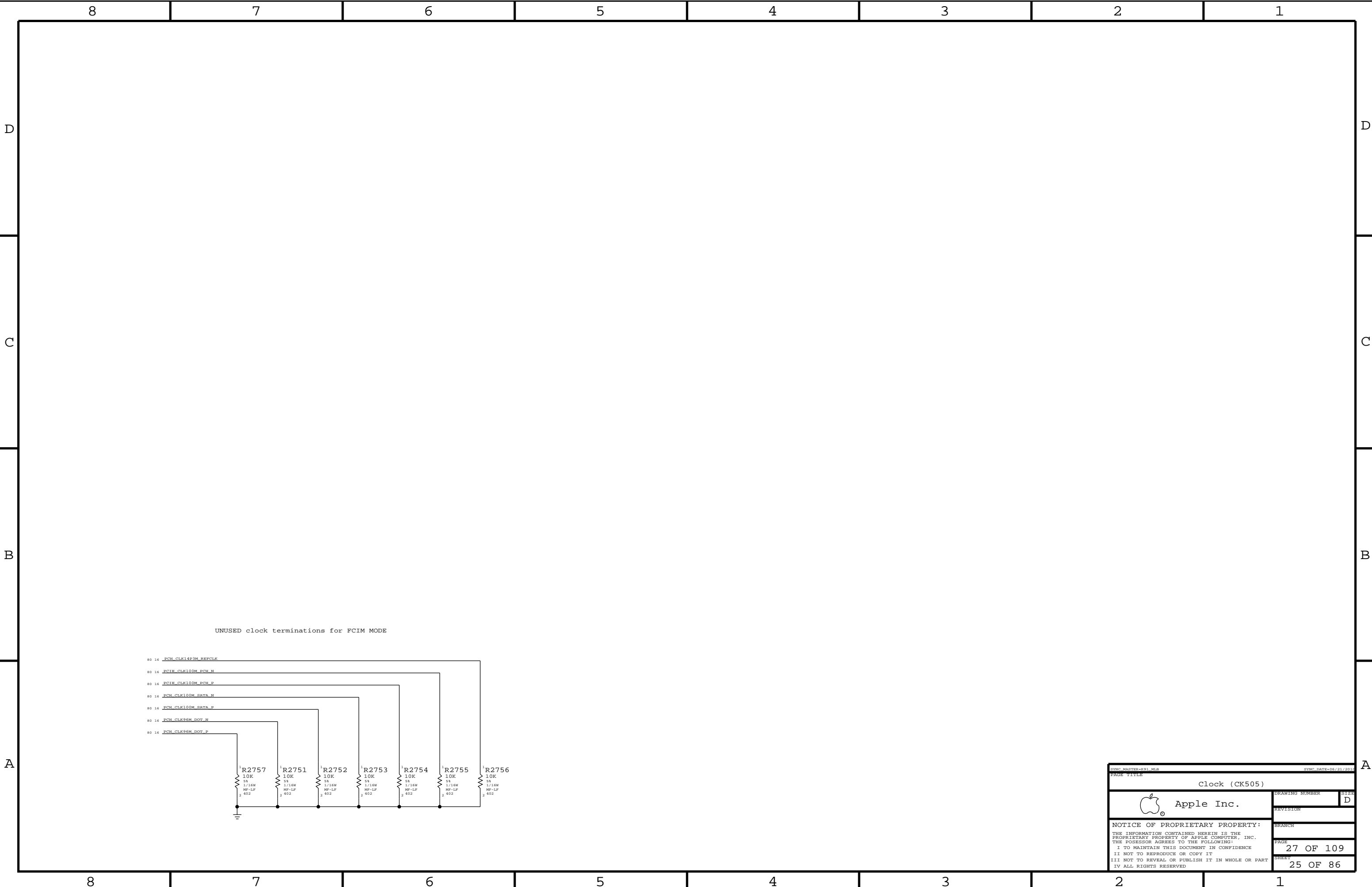
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UNUSED clock terminations for FCIM MODE

SYNOPSIS: CK505.MBR

SYNOPSIS: CK505.MBR

Clock (CK505)

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System RTC Power Source & 32kHz / 25MHz Clock Generator

Platform Reset Connections

Unbuffered

Buffered

ENET_MEDIA_SENSE ISOLATION CIRCUIT

Ethernet WAKE# Isolation


PCH S0 PWRGD

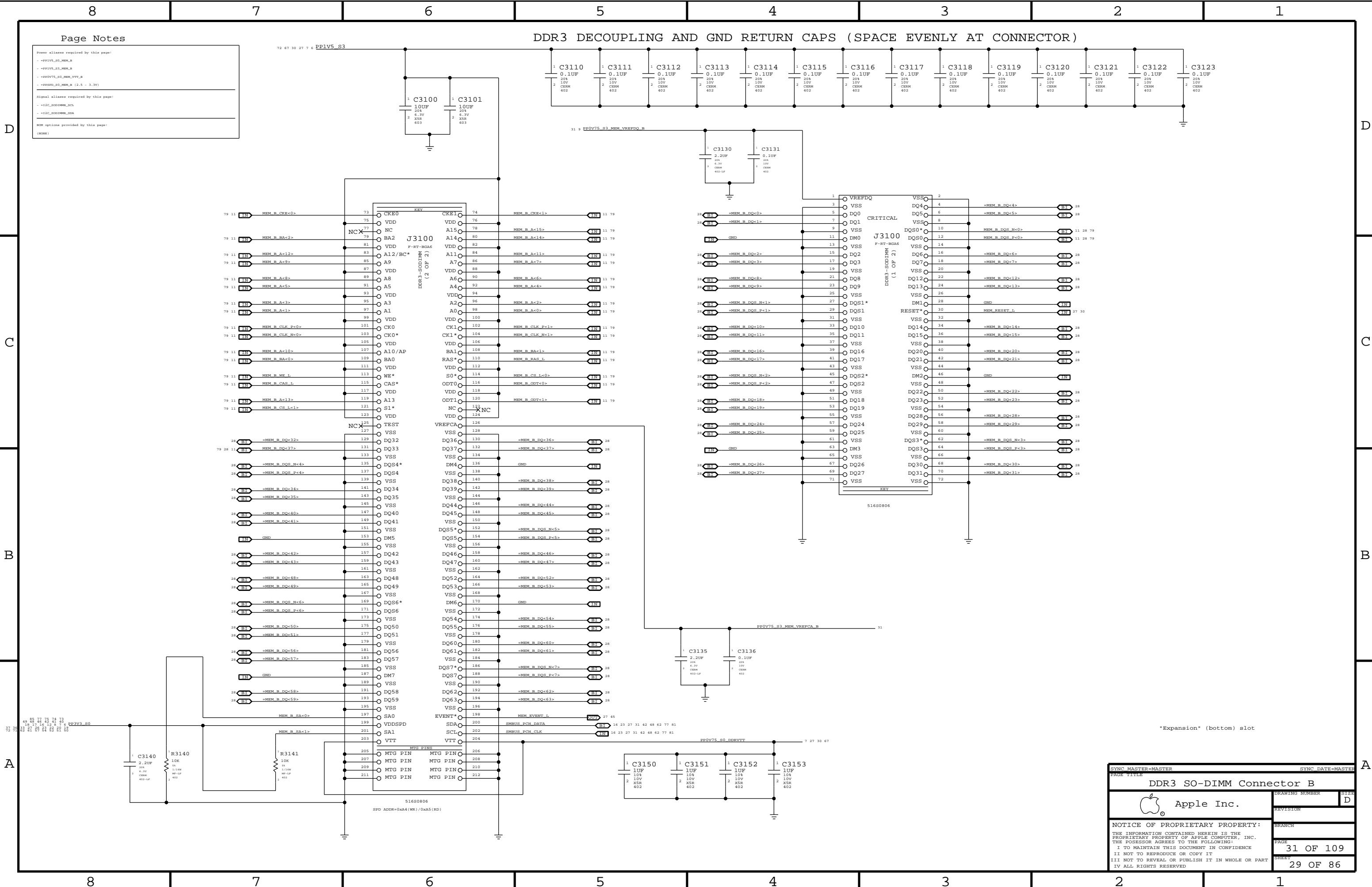
PCH Reset Button

PAGE TITLE		SYNC MASTER=LINDA K901		SYNC DATE=07/08/2010	
Chipset Support		DRAWING NUMBER		SIZE	
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8	7	6	5	4	3	2	1
D	CPU CHANNEL A DQS 0 -> DIMM A DQS 0		CPU CHANNEL B DQS 0 -> DIMM B DQS 0				
	79 28 27 11	MEM A DQS N<0>	11 27 28 79 79 28 27 11	MEM B DQS N<0>	11 28 29 79		
	79 28 27 11	MEM A DQS P<0>	11 27 28 79 79 28 27 11	MEM B DQS P<0>	11 28 29 79		
		MAKE_BASE=TRUE		MAKE_BASE=TRUE			
	79 11	MEM A DQ<7>	27	79 11	MEM B DQ<7>	29	
	79 11	MEM A DQ<6>	27	79 11	MEM B DQ<6>	29	
	79 11	MEM A DQ<5>	27	79 11	MEM B DQ<5>	29	
	79 11	MEM A DQ<4>	27	79 11	MEM B DQ<4>	29	
	79 11	MEM A DQ<3>	27	79 11	MEM B DQ<3>	29	
C	CPU CHANNEL A DQS 1 -> DIMM A DQS 1		CPU CHANNEL B DQS 1 -> DIMM B DQS 1				
	79 11	MEM A DQS N<1>	27	79 11	MEM B DQS N<1>	29	
	79 11	MEM A DQS P<1>	27	79 11	MEM B DQS P<1>	29	
		MAKE_BASE=TRUE			MAKE_BASE=TRUE		
	79 11	MEM A DQ<15>	27	79 11	MEM B DQ<15>	29	
	79 11	MEM A DQ<14>	27	79 11	MEM B DQ<14>	29	
	79 11	MEM A DQ<13>	27	79 11	MEM B DQ<13>	29	
	79 11	MEM A DQ<12>	27	79 11	MEM B DQ<12>	29	
	79 11	MEM A DQ<11>	27	79 11	MEM B DQ<11>	29	
B	CPU CHANNEL A DQS 2 -> DIMM A DQS 2		CPU CHANNEL B DQS 2 -> DIMM B DQS 2				
	79 11	MEM A DQS N<2>	27	79 11	MEM B DQS N<2>	29	
	79 11	MEM A DQS P<2>	27	79 11	MEM B DQS P<2>	29	
		MAKE_BASE=TRUE			MAKE_BASE=TRUE		
	79 11	MEM A DQ<23>	27	79 11	MEM B DQ<23>	29	
	79 11	MEM A DQ<22>	27	79 11	MEM B DQ<22>	29	
	79 11	MEM A DQ<21>	27	79 11	MEM B DQ<21>	29	
	79 11	MEM A DQ<20>	27	79 11	MEM B DQ<20>	29	
	79 11	MEM A DQ<19>	27	79 11	MEM B DQ<19>	29	
A	CPU CHANNEL A DQS 3 -> DIMM A DQS 3		CPU CHANNEL B DQS 3 -> DIMM B DQS 3				
	79 11	MEM A DQS N<3>	27	79 11	MEM B DQS N<3>	29	
	79 11	MEM A DQS P<3>	27	79 11	MEM B DQS P<3>	29	
		MAKE_BASE=TRUE			MAKE_BASE=TRUE		
	79 11	MEM A DQ<31>	27	79 11	MEM B DQ<31>	29	
	79 11	MEM A DQ<30>	27	79 11	MEM B DQ<30>	29	
	79 11	MEM A DQ<29>	27	79 11	MEM B DQ<29>	29	
	79 11	MEM A DQ<28>	27	79 11	MEM B DQ<28>	29	
	79 11	MEM A DQ<27>	27	79 11	MEM B DQ<27>	29	

NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

SYNC MASTER=ANNE K901		SYNC DATE=06/22/2010	
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DDR3 Byte/Bit Swaps			
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Page Notes

Power aliases required by this page:

- ~PP1V5_S3_MEM_B
- ~PP1V5_S3_MEM_B
- ~PP0V75_S3_MEM_VTT_B
- ~PPSPD_S3_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- ~I2C_S0D1MMB_SCL
- ~I2C_S0D1MMB_SDA

ROM options provided by this page:

(None)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

"Expansion" (bottom) slot

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SO-DIMM Connector B			
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

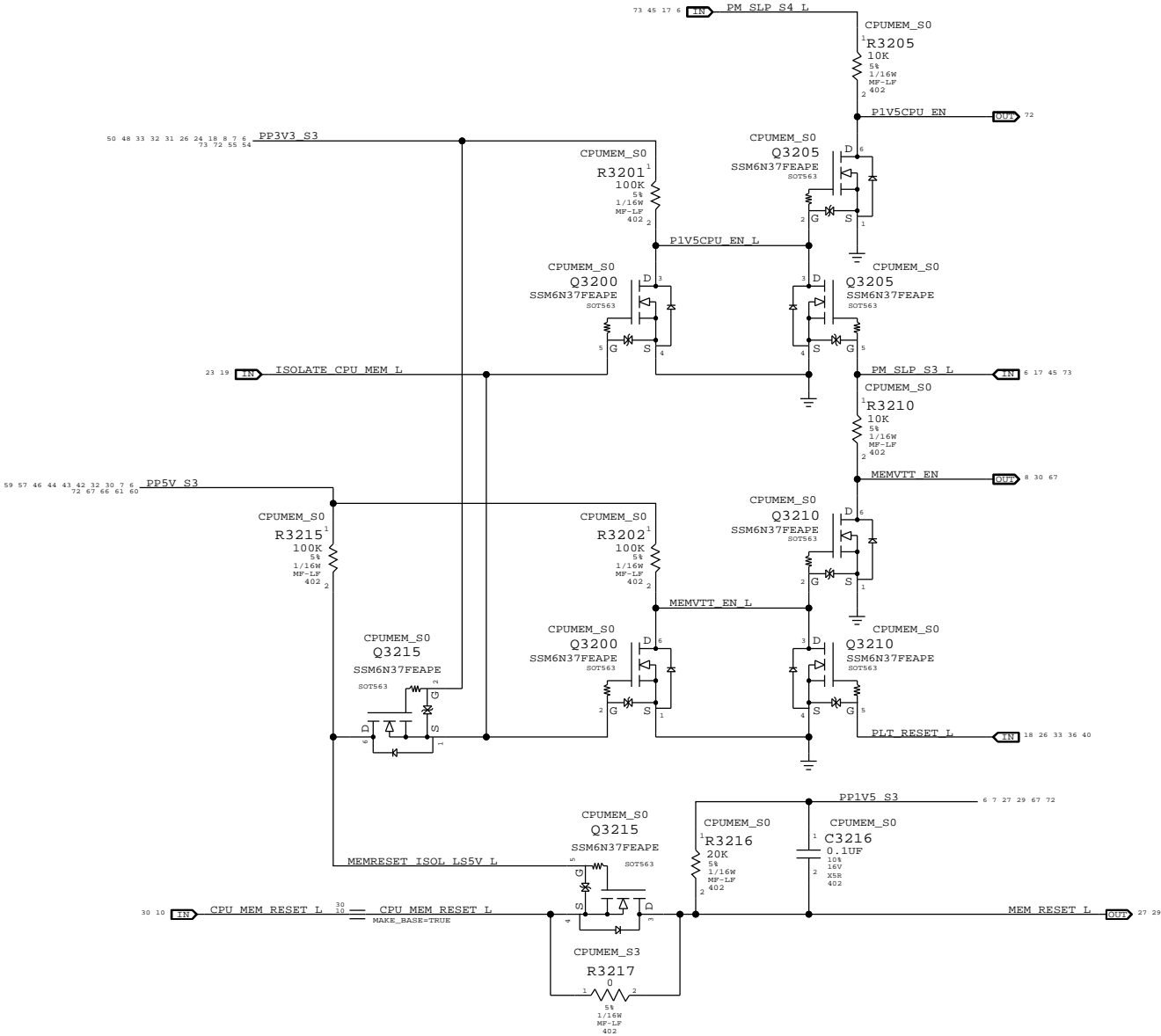
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

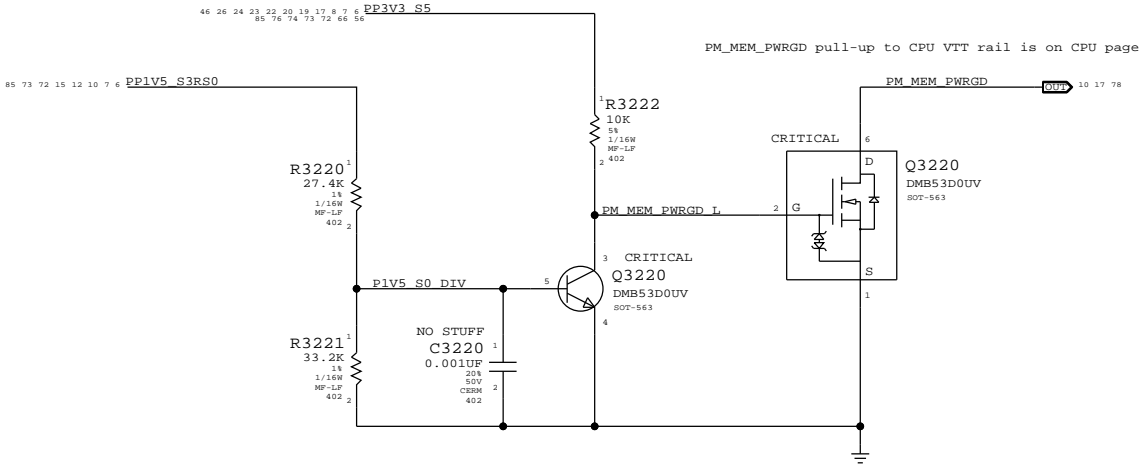
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

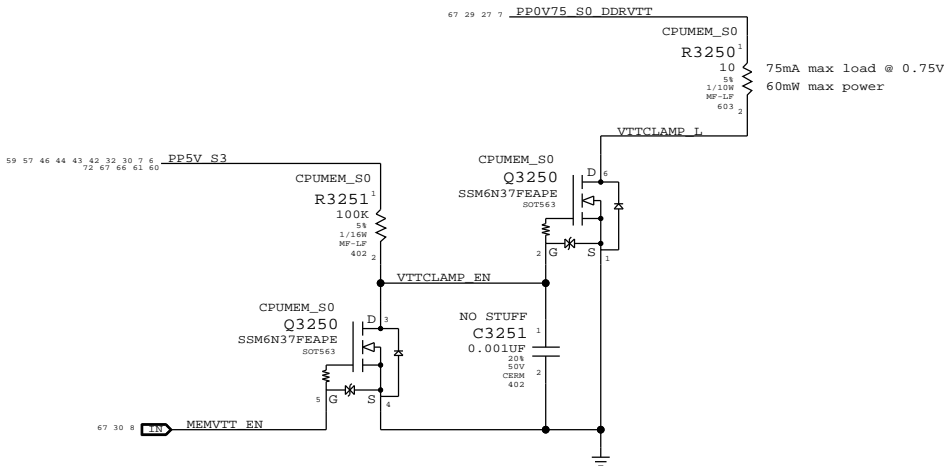


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp


Ensures CKE signals are held low in S3

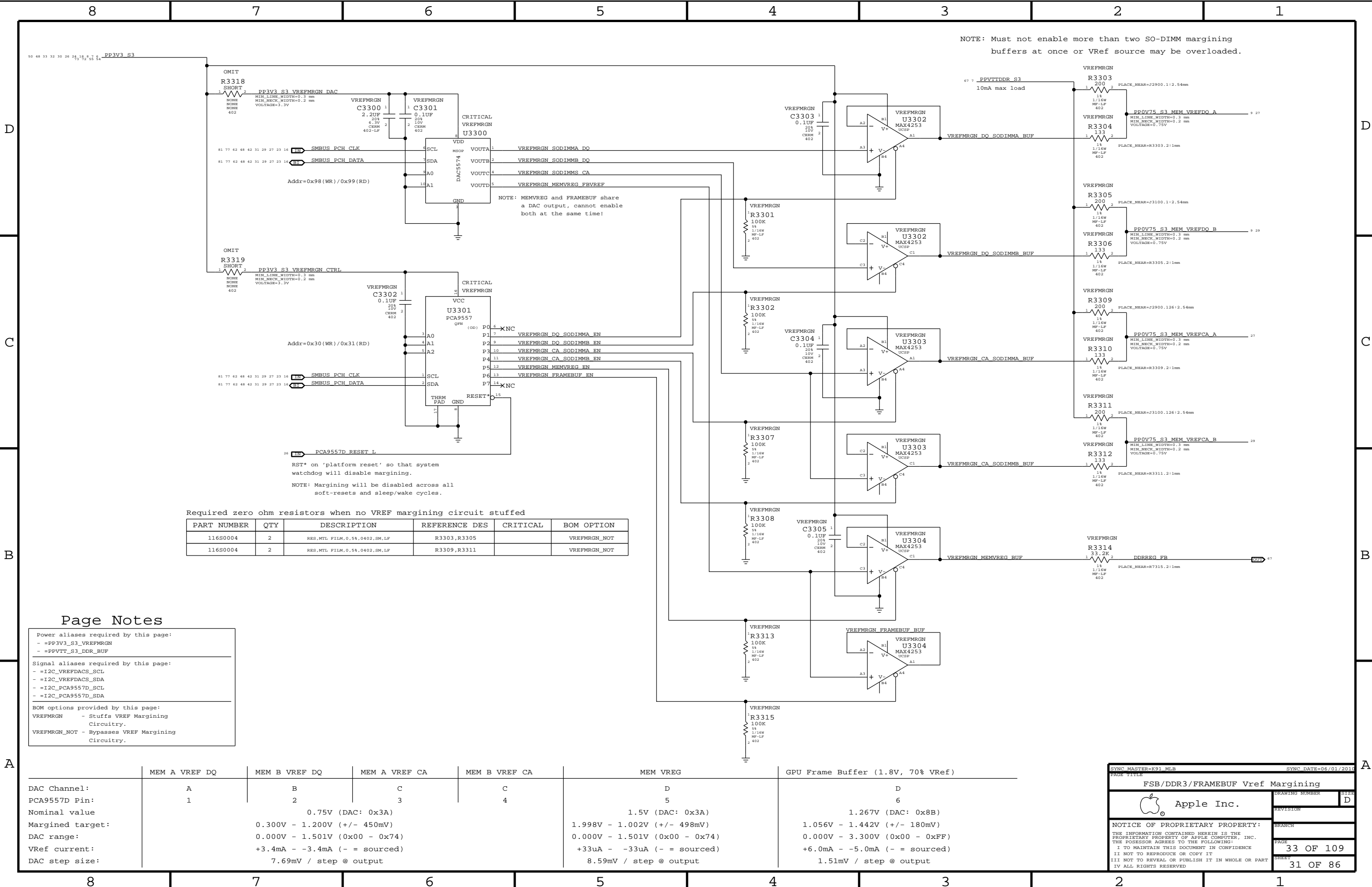


Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=ANNE K901		SYNC DATE=06/22/2010	
PAGE TITLE			
CPU Memory S3 Support			
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Page Notes

Power aliases required by this page:

- PP3V3_S3_VREFMRGN
- PPVTT_S3_DDR_BUF

Signal aliases required by this page:

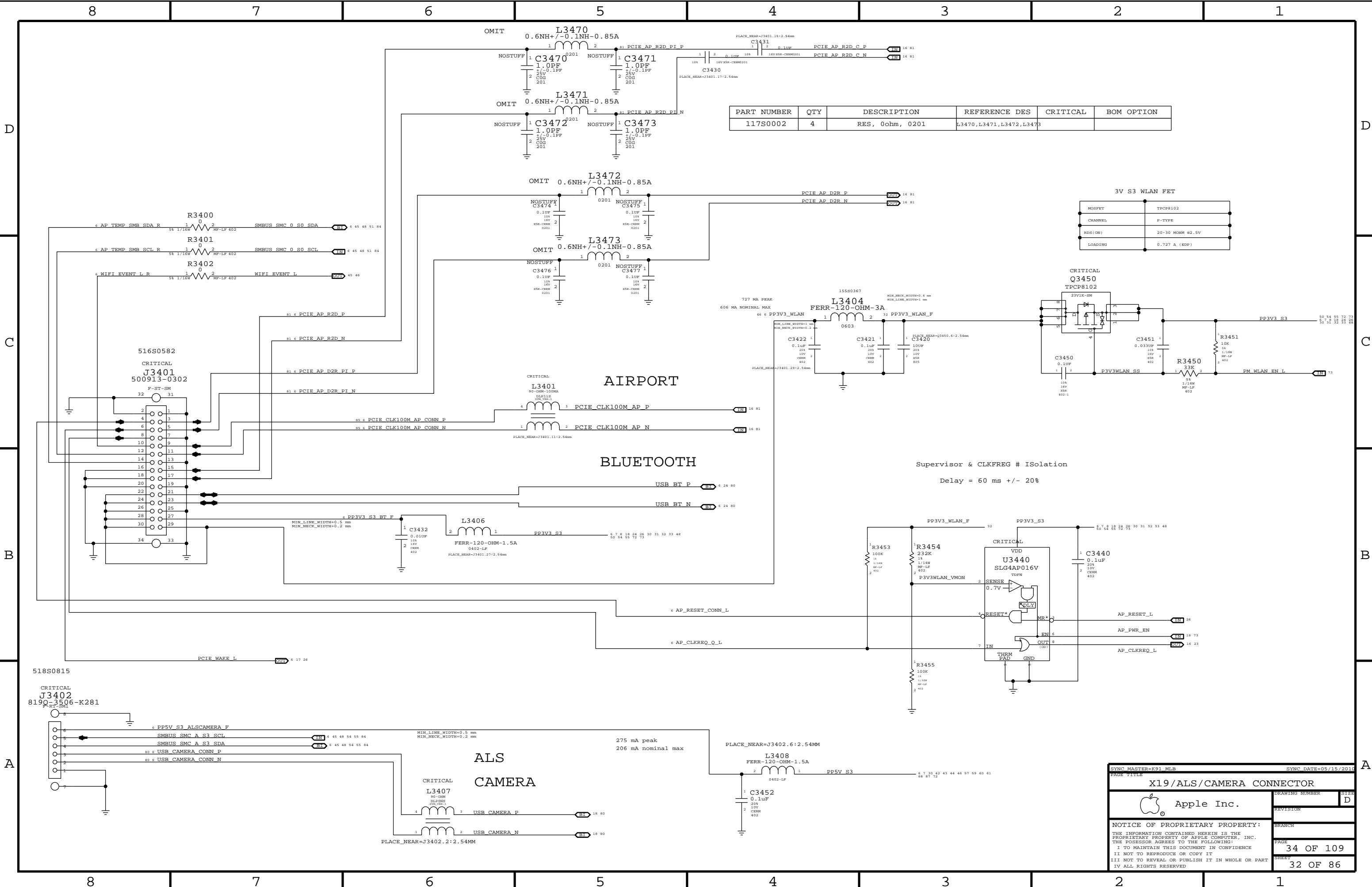
- I2C_VREFDACS_SCL
- I2C_VREFDACS_SDA
- I2C_PCA9557D_SCL
- I2C_PCA9557D_SDA

BOM options provided by this page:

- VREFMRGN - Stuffs VREF Margining Circuitry.
- VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

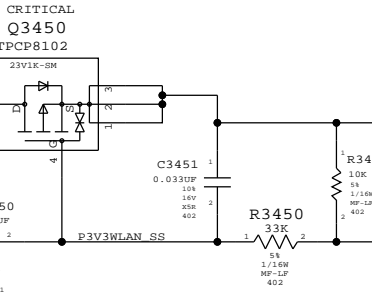
	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

PAGE TITLE		SYNC DATE=06/01/2010	
FSB/DDR3/FRAMEBUF Vref Margining		DRAWING NUMBER	SIZE
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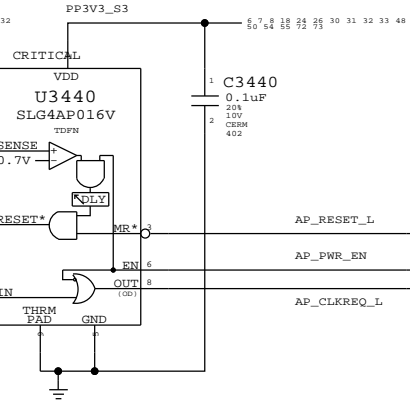


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470, L3471, L3472, L3473		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (RDP)



Supervisor & CLKFREQ # Isolation
Delay = 60 ms +/- 20%



SYNC MASTER=K91 MLB		SYNC DATE=05/15/2010	
PAGE TITLE		X19/ALS/CAMERA CONNECTOR	
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D

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A

D

C

B

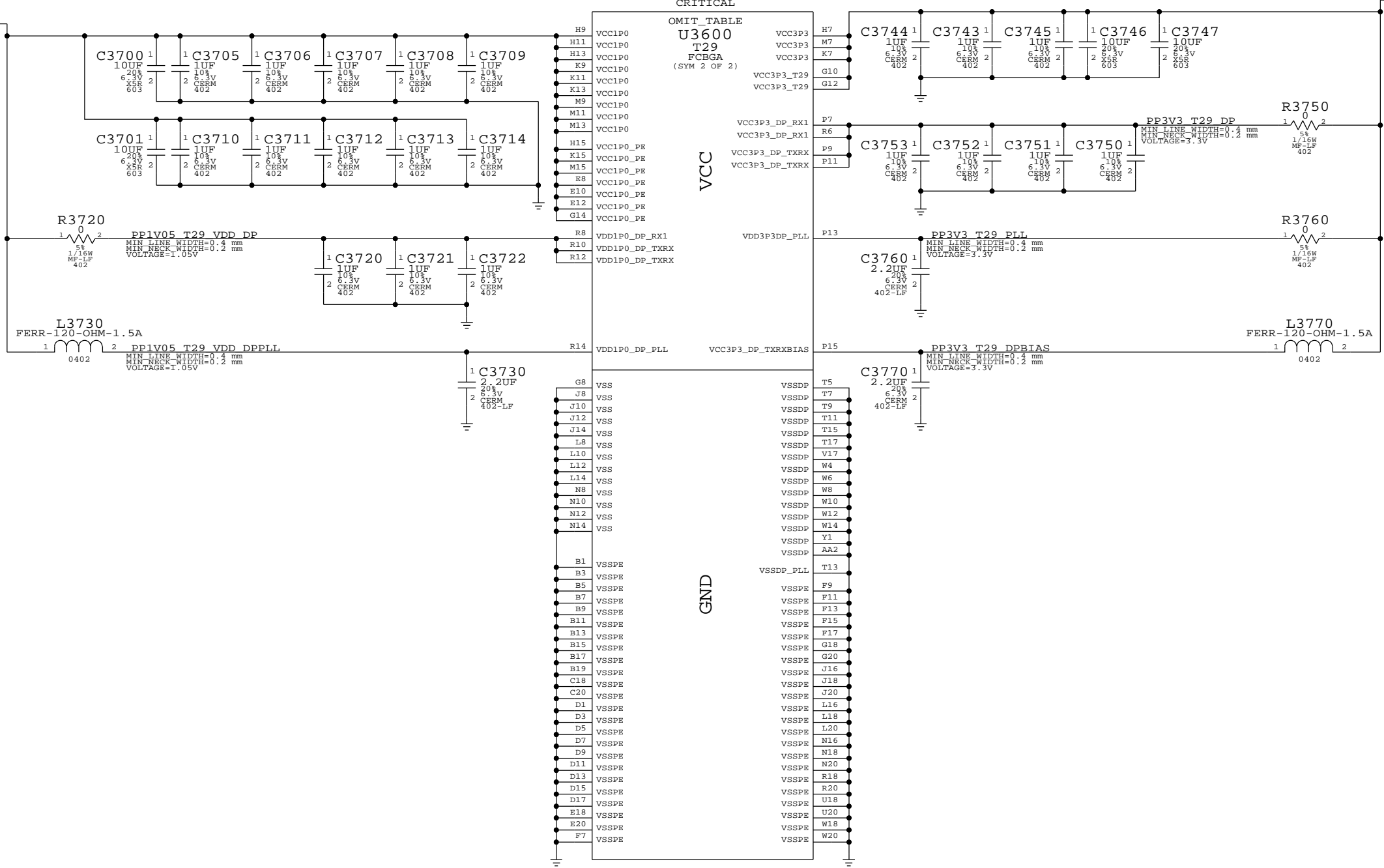
A

8 7 6 5 4 3 2 1

36 7 PP1V05 T29
2100 mA (Single Port)
2250 mA (Dual Port)
EDP: 3000 mA

PP3V3 T29 7 16 19 26 34 36
135 mA (Single-Port)
152 mA (Dual-Port)
EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=T29		SYNC DATE=10/12/2010	
PAGE TITLE			
T29 Host (2 of 2)			
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8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:

- PPVIN_SW_T29BST (8-13V Boost Input)
- PP18V_T29_REG (18V Boost Output)
- PP3V3_T29_P3V3T29FET (3.3V FET Input)
- PP3V3_T29_FET (3.3V FET Output)
- PP3V3_S0_T29PWRCTL
- PP1V05_T29_P1V05T29FET (1.05V FET Input)
- PP1V05_T29_FET (1.05V FET Output)

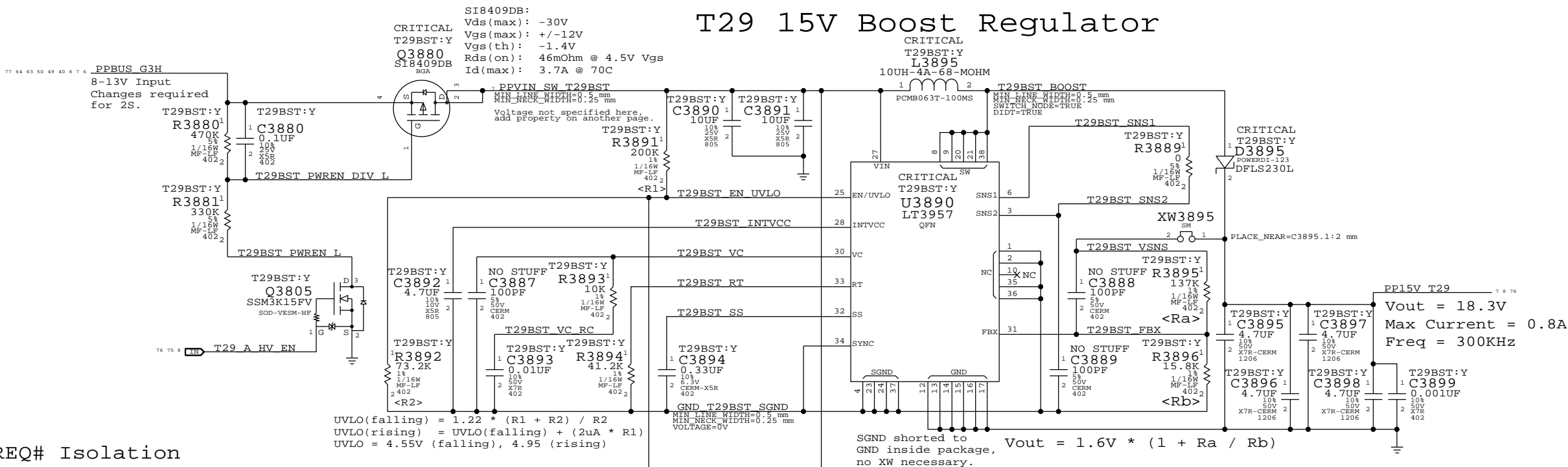
Signal aliases required by this page:

- T29_CLKREQ_L
- T29_RESET_L

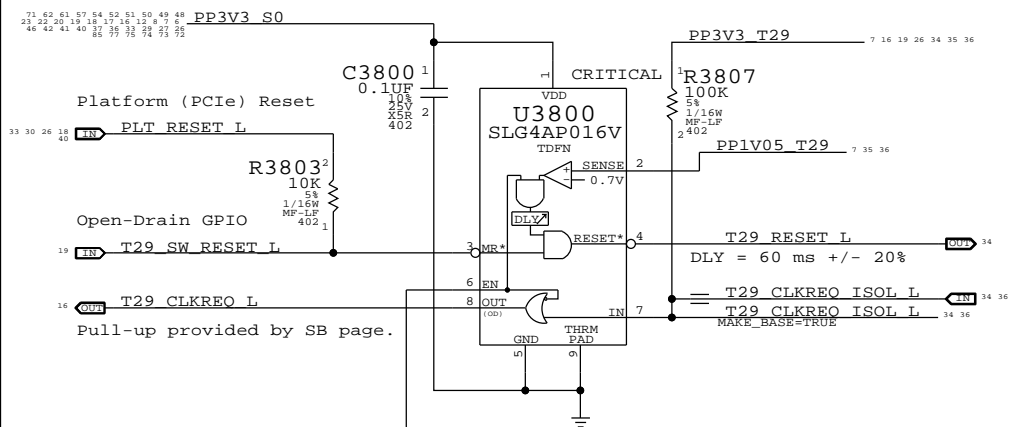
BOM options provided by this page:

T29BST:Y - Stuffs 18V boost circuitry.

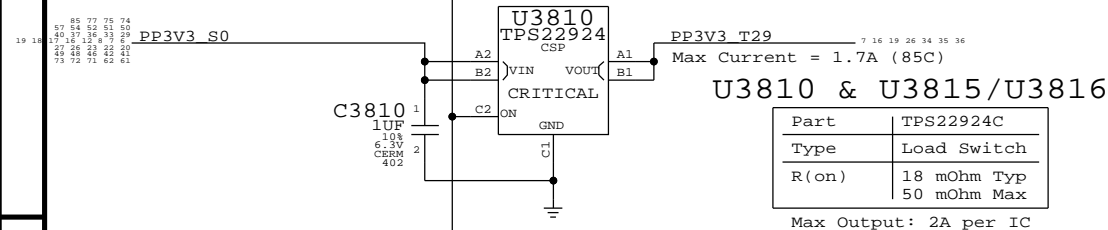
T29 15V Boost Regulator



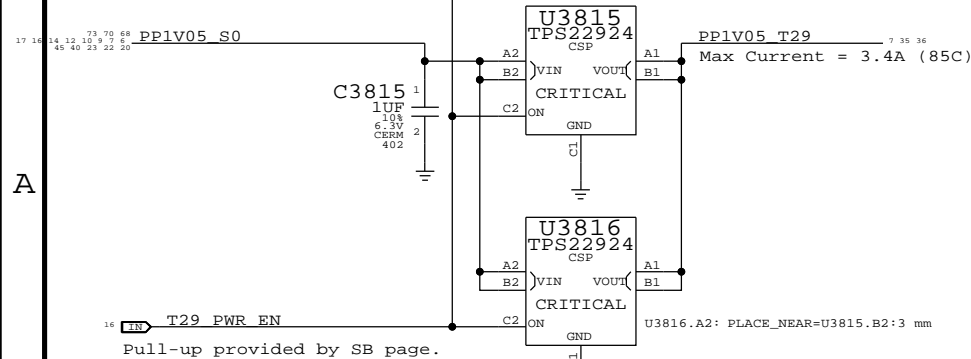
Supervisor & CLKREQ# Isolation



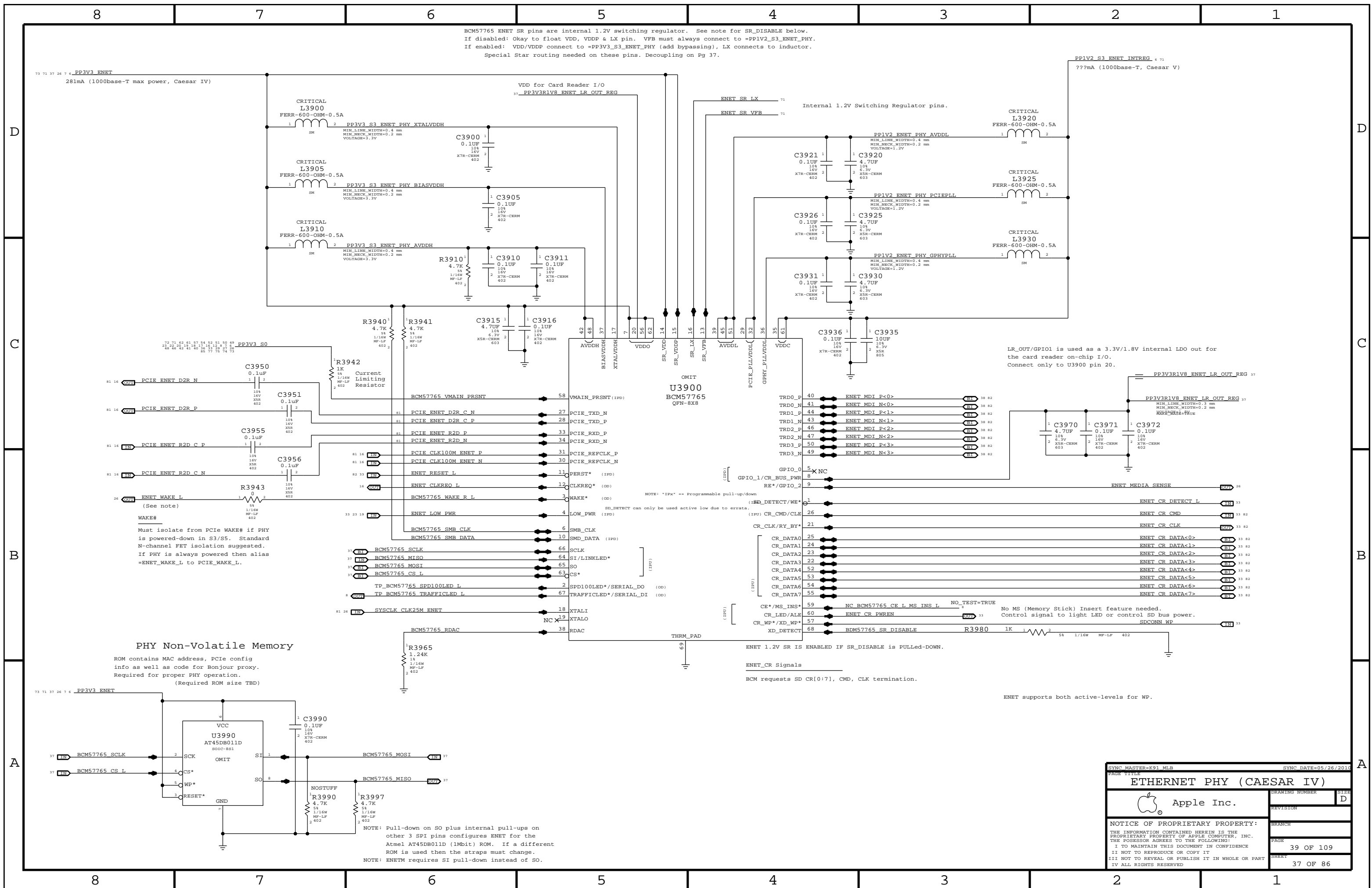
3.3V T29 Switch



1.05V T29 Switch



SYNC MASTER=T29		SYNC DATE=10/12/2010	
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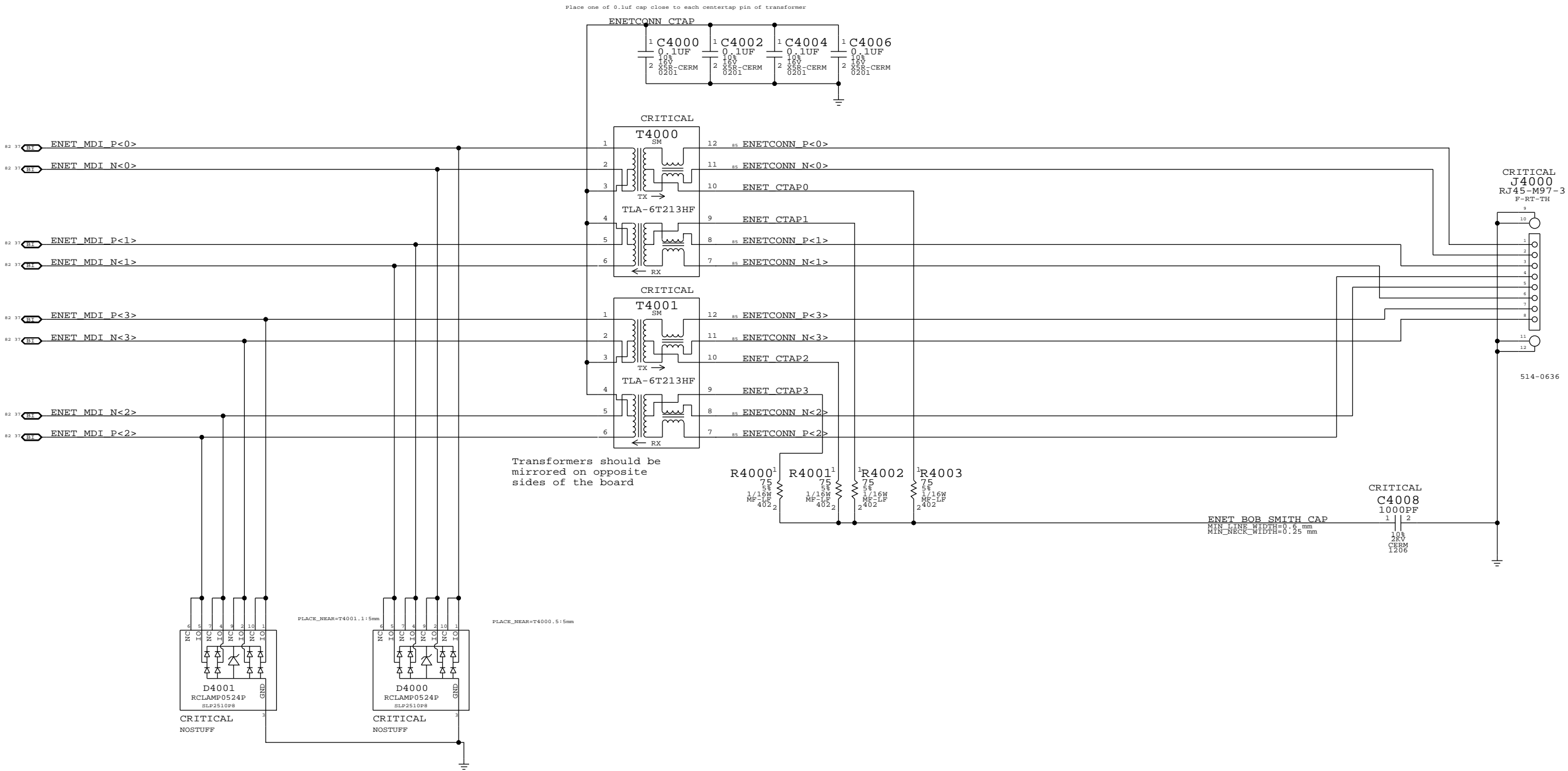



Page Notes

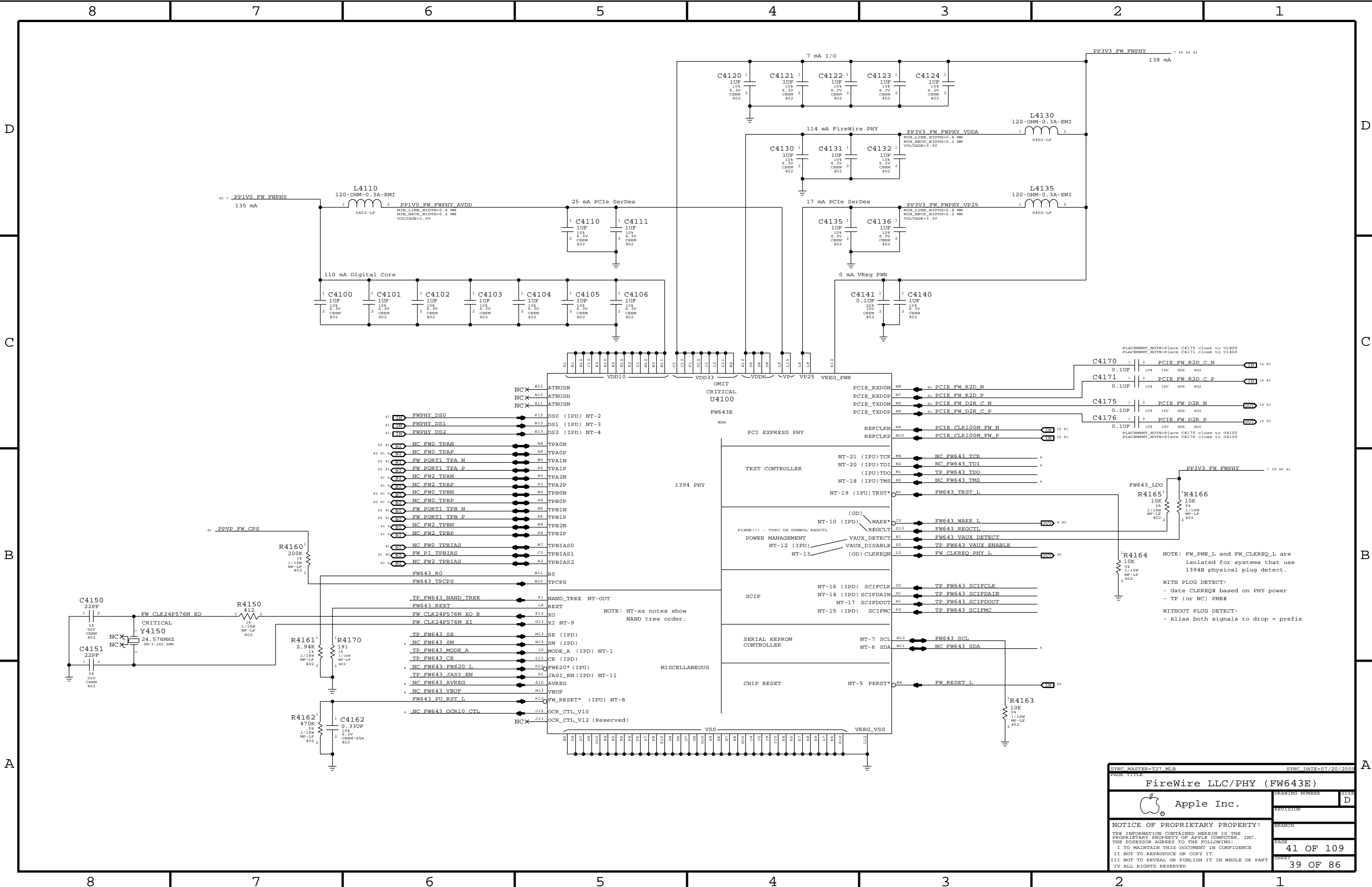
Power aliases required by this page:
(NONE)


Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91 MLB		SYNC DATE=05/26/2010	
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Ethernet Connector			
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SYNC MASTER=T27 MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
FireWire LLC/PHY (FW643E)			
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Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

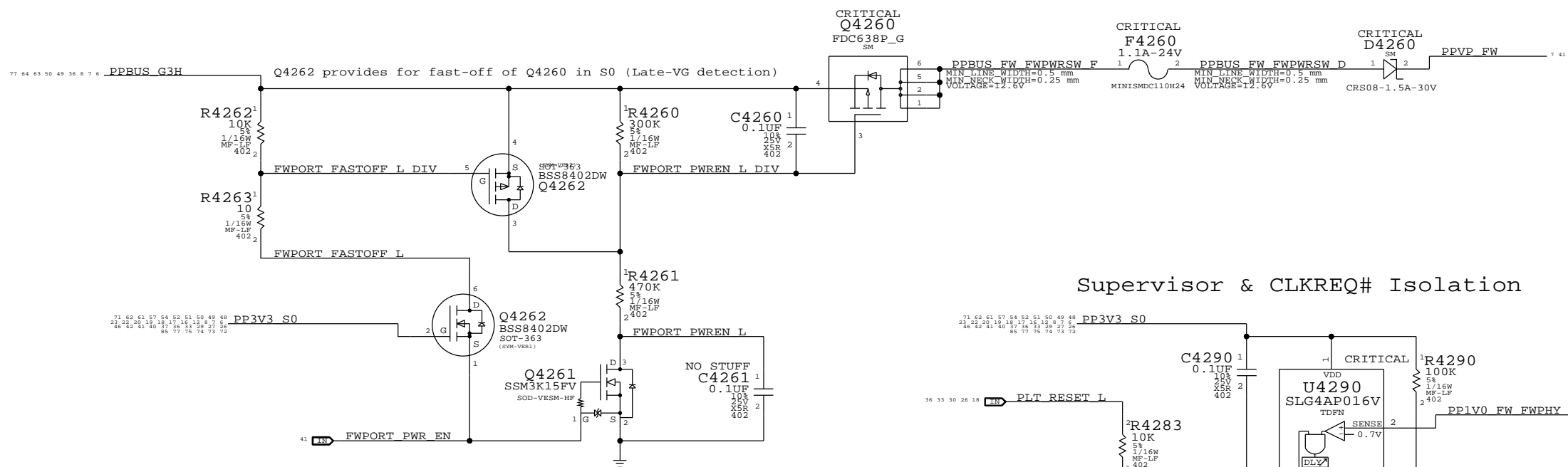
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

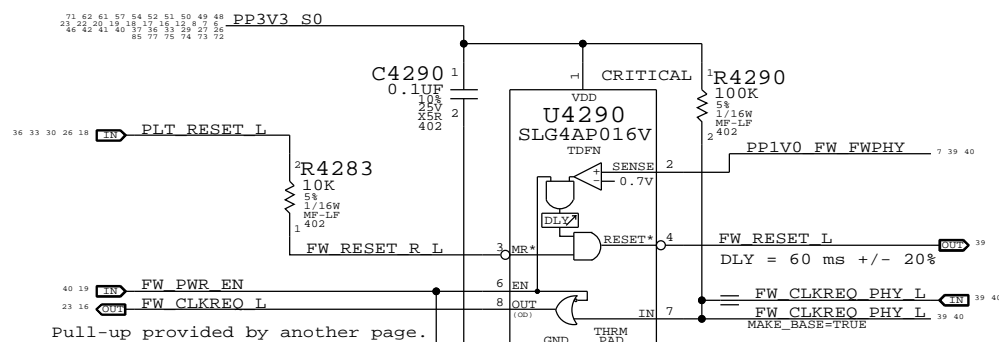
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

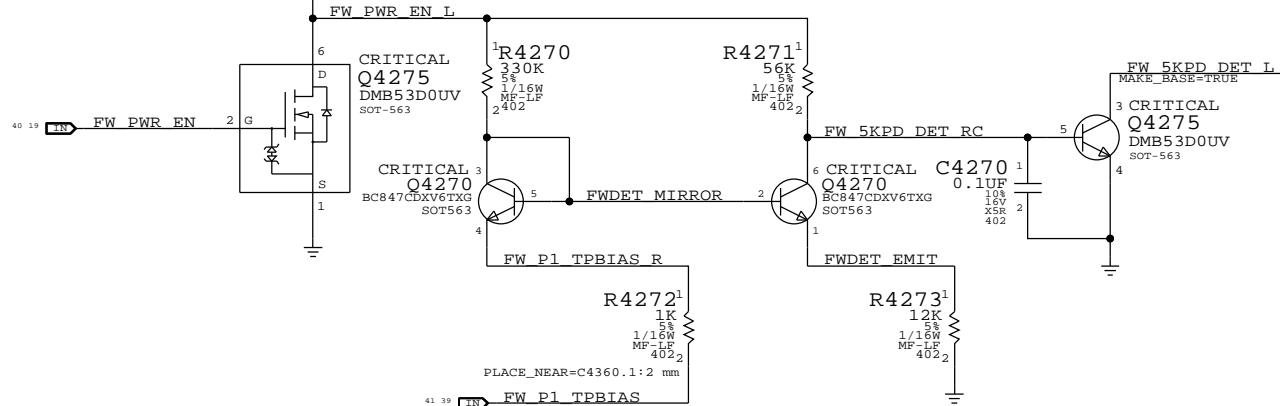


Supervisor & CLKREQ# Isolation



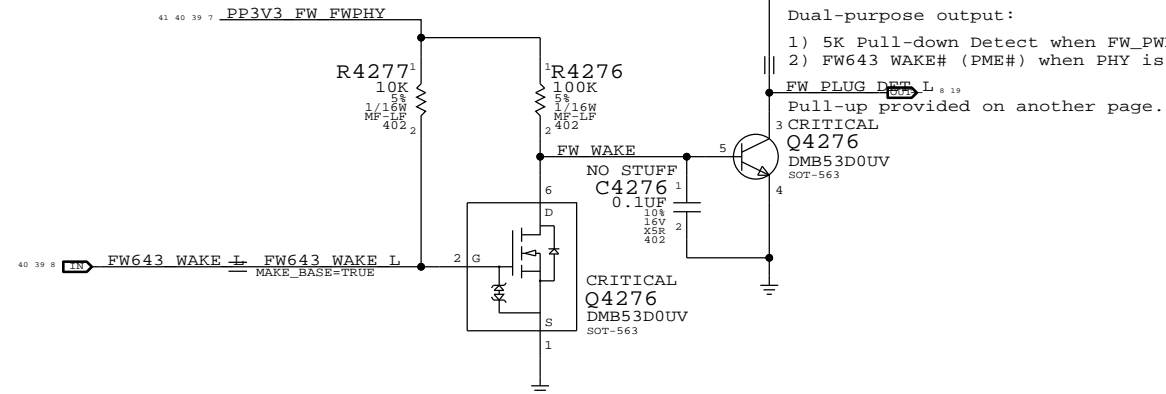
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

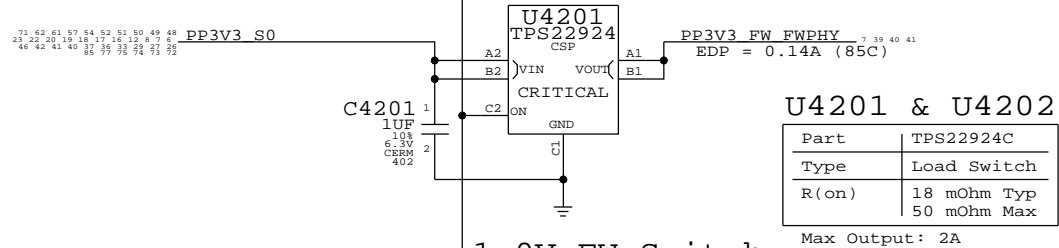


Dual-purpose output:

- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

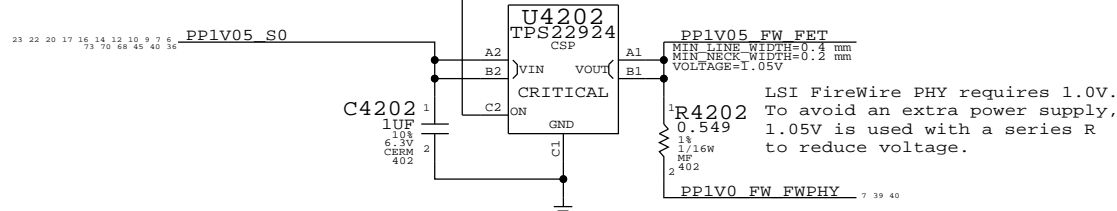
3.3V FW Switch



Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=T27_MLB		SYNC DATE=12/15/2009	
PAGE TITLE		FireWire Port & PHY Power	
Apple Inc.		DRAWING NUMBER	SIZE D
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Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

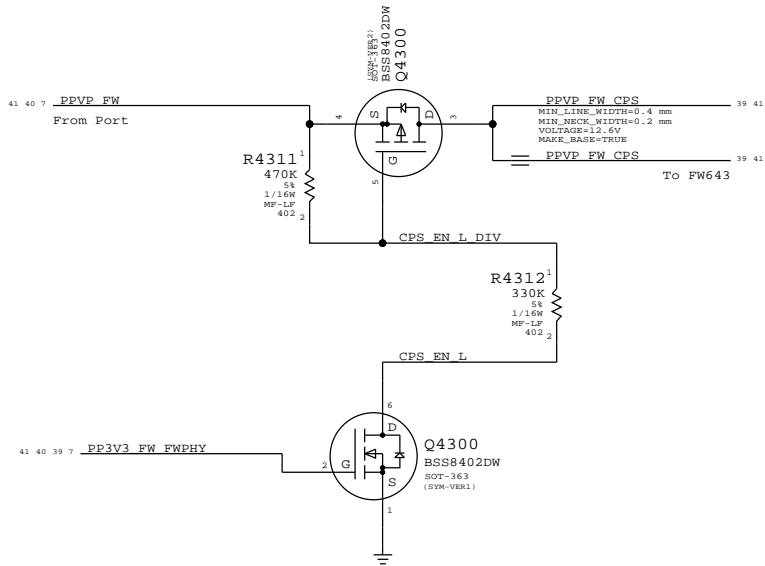
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:

(NONE)
1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

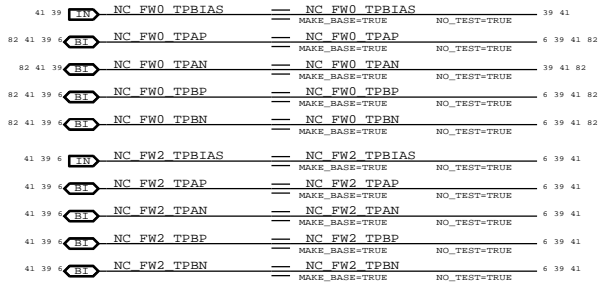
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



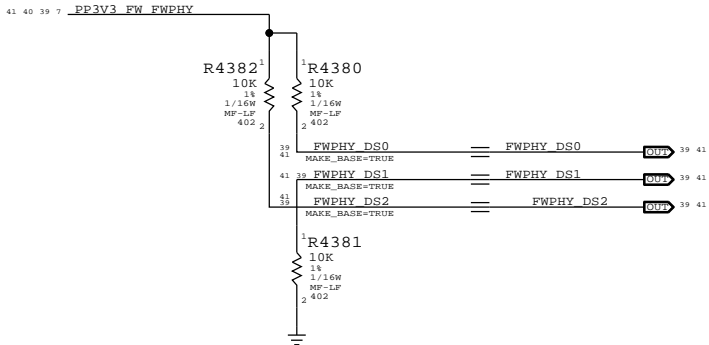
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



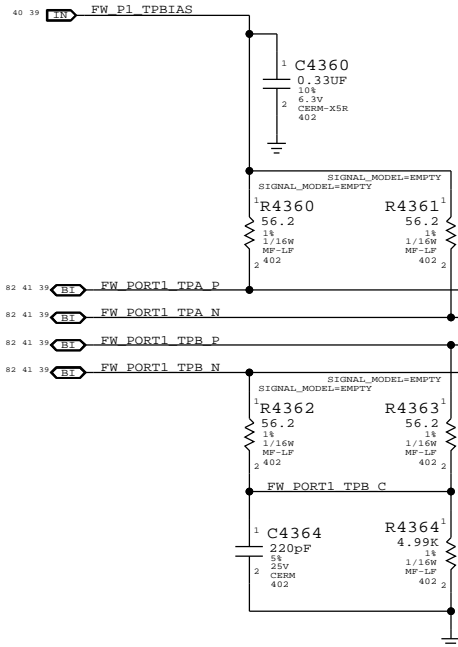
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



Termination

Place close to FireWire PHY



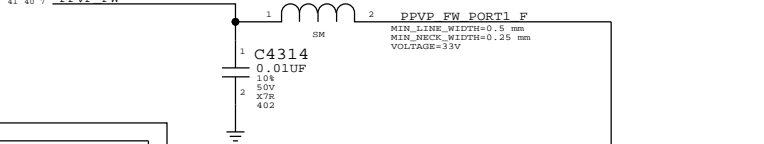
Cable Power

CRITICAL

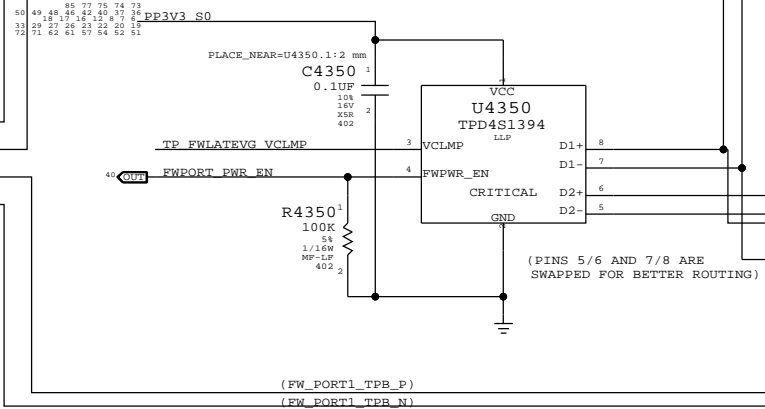
L4310

FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A



"Snapback" & "Late VG" Protection



PORT 1

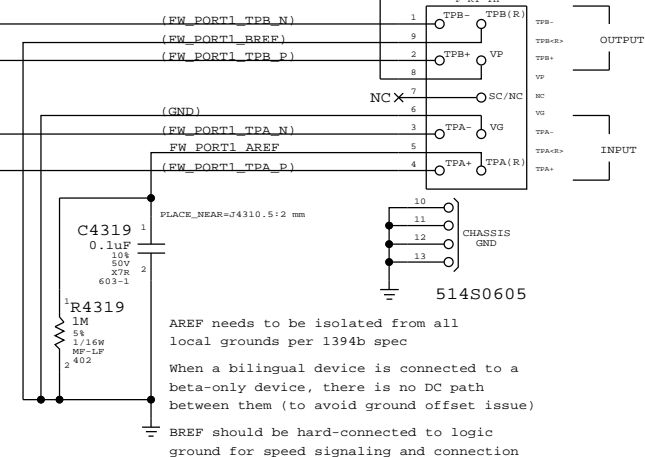
BILINGUAL

CRITICAL

J4310

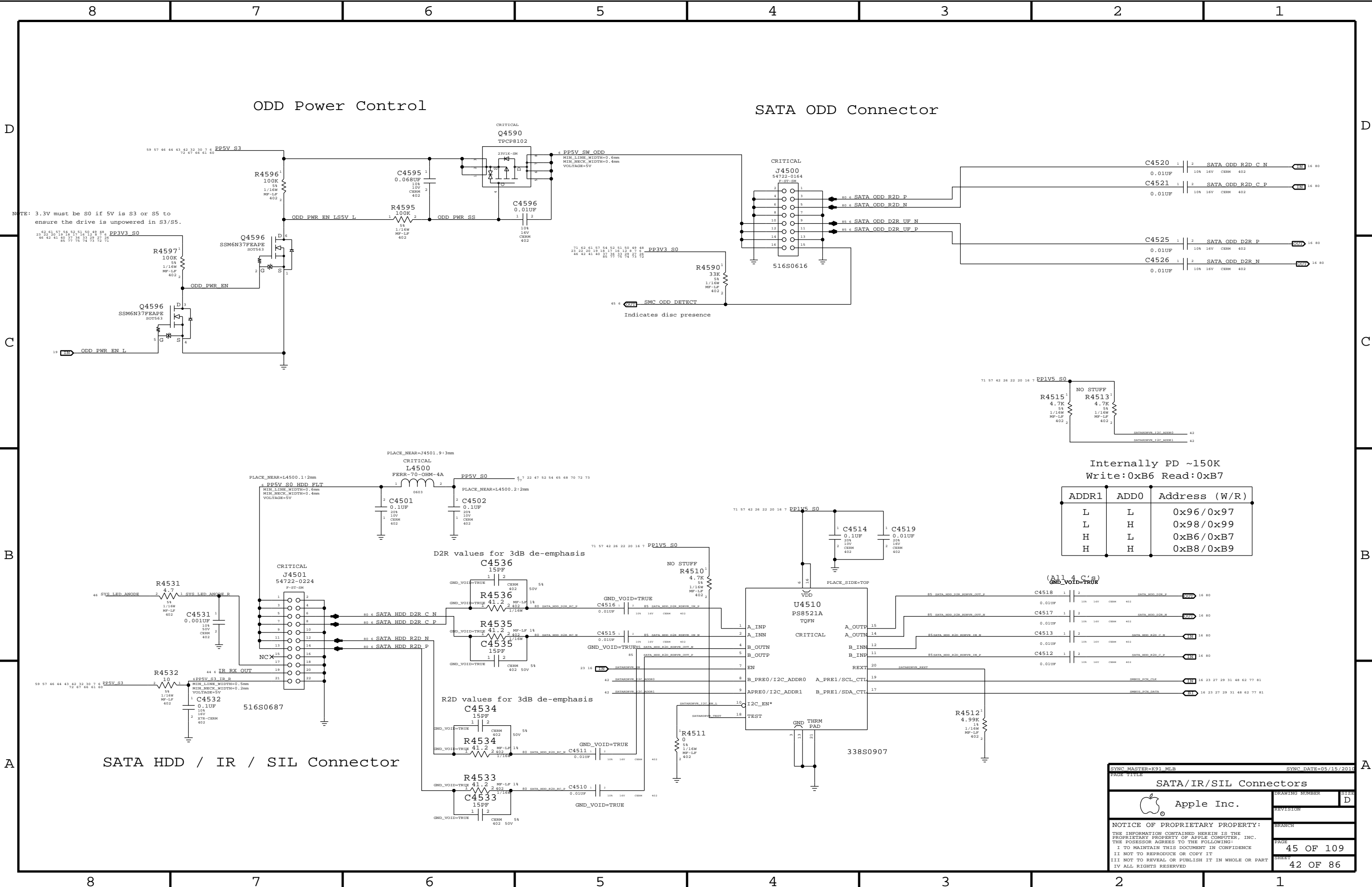
1394B-M97

F-RT-TH



AREF needs to be isolated from all local grounds per 1394b spec
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED



Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (W/R)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SYNC MASTER=K91 MLB

SYNC DATE=05/15/2010

SATA/IR/SIL Connectors

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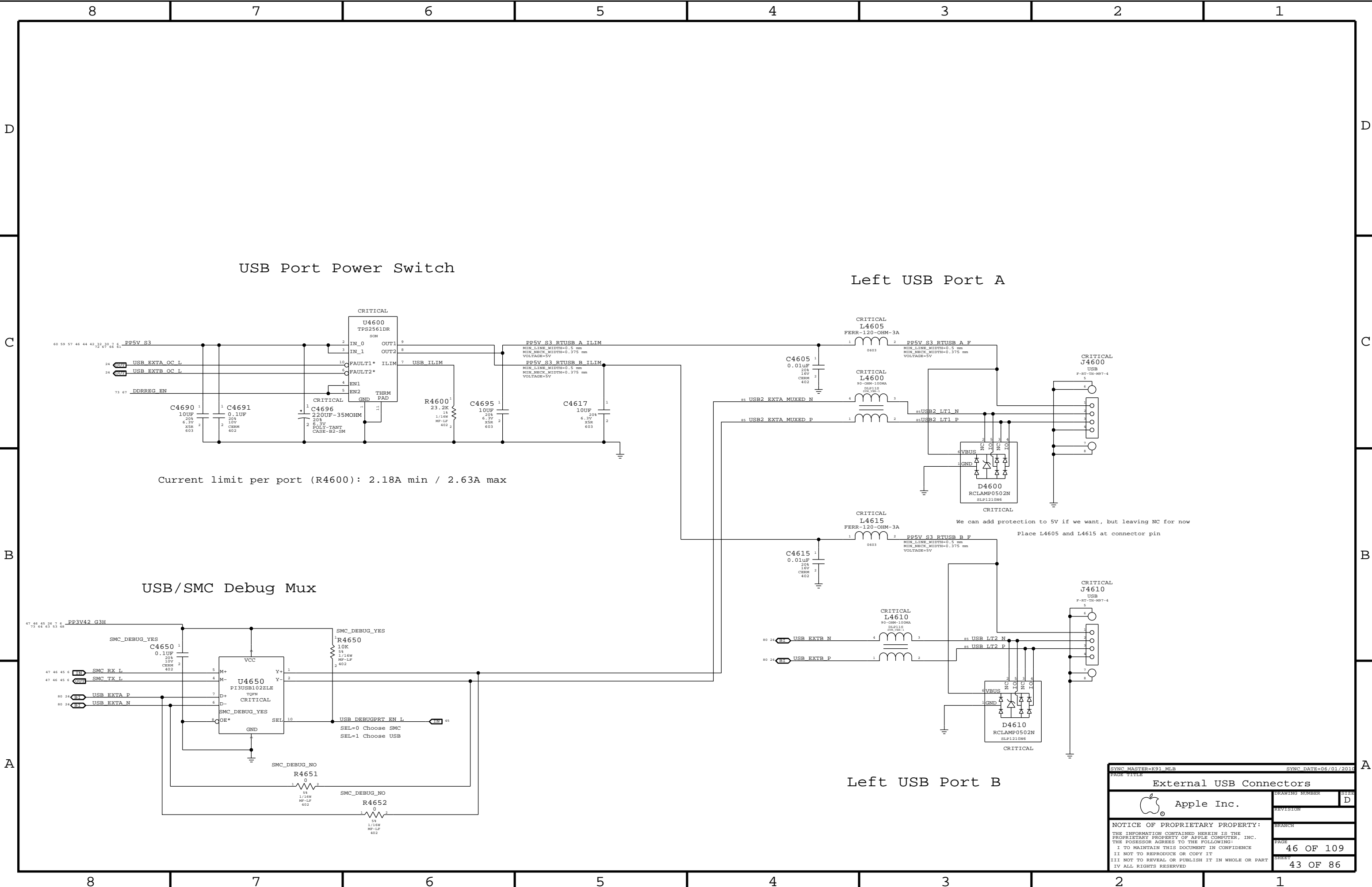
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
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SYNC MASTER=K91 MLB		SYNC DATE=06/01/2010	
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External USB Connectors		DRAWING NUMBER	SIZE
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IR SUPPORT

The schematic diagram illustrates the IR support circuitry centered around the U4800 IC (CY7C63803-LQXC QPS). The IC is connected to various components as follows:

- VCC:** Connected to PP5V_S3.
- C4801:** A 0.1uF capacitor connected between VCC and ground.
- USB_IR_P and USB_IR_N:** Differential pair inputs connected to pins P1.0/D+ and P1.1/D- respectively.
- IR_VREF_FILTER:** Connected to pin P1.2/VREG.
- C4803:** A 1uF capacitor connected between the IR_VREF_FILTER input and ground.
- Pins P1.3/SSEL, P1.4/SCLK, P1.5/SMOSI, and P1.6/SMISO:** These pins are connected to internal functions: INT0/P0.2, INT1/P0.3, INT2/P0.4, TIO0/P0.5, and TIO1/P0.6 respectively.
- CRITICAL OMIT:** Pins 8 through 24 are labeled as CRITICAL OMIT.
- THRML_PAD:** Thermal pad connected to VSS.
- R4800:** A 100 ohm resistor connected between pin 2 (IR_RX_OUT_RC) and pin 6 (IR_RX_OUT).
- C4804:** A 0.001uF capacitor connected between pin 2 and ground.

Component Details:

- C4801:** 0.1uF, 10V, X7R-CERM, 402
- C4803:** 1uF, 10V, X5S, 402-1
- C4804:** 0.001uF, 10V, CERM, 402
- R4800:** 100 ohms, 5%, 1/16W, MF-LP, 402

U4800 Pinout:

Pin	Signal	Internal Function
7	P0.0	
8	P0.1	
9	P0.2	INT0/P0.2
10	P0.3	INT1/P0.3
11	P0.4	INT2/P0.4
12	P1.0/D+	
13	P1.1/D-	
14	P1.2/VREG	
15	P1.3/SSEL	INT0/P0.2
16	P1.4/SCLK	INT1/P0.3
17	P1.5/SMOSI	TIO0/P0.5
18	P1.6/SMISO	TIO1/P0.6
19		
20		
21		
22		
23		
24		

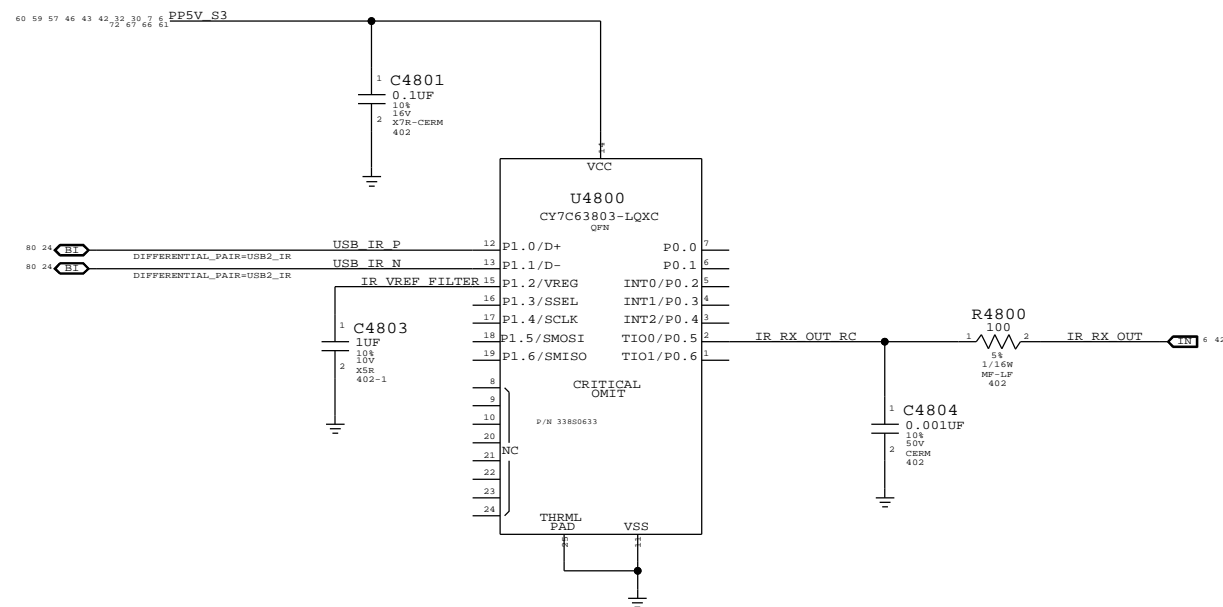
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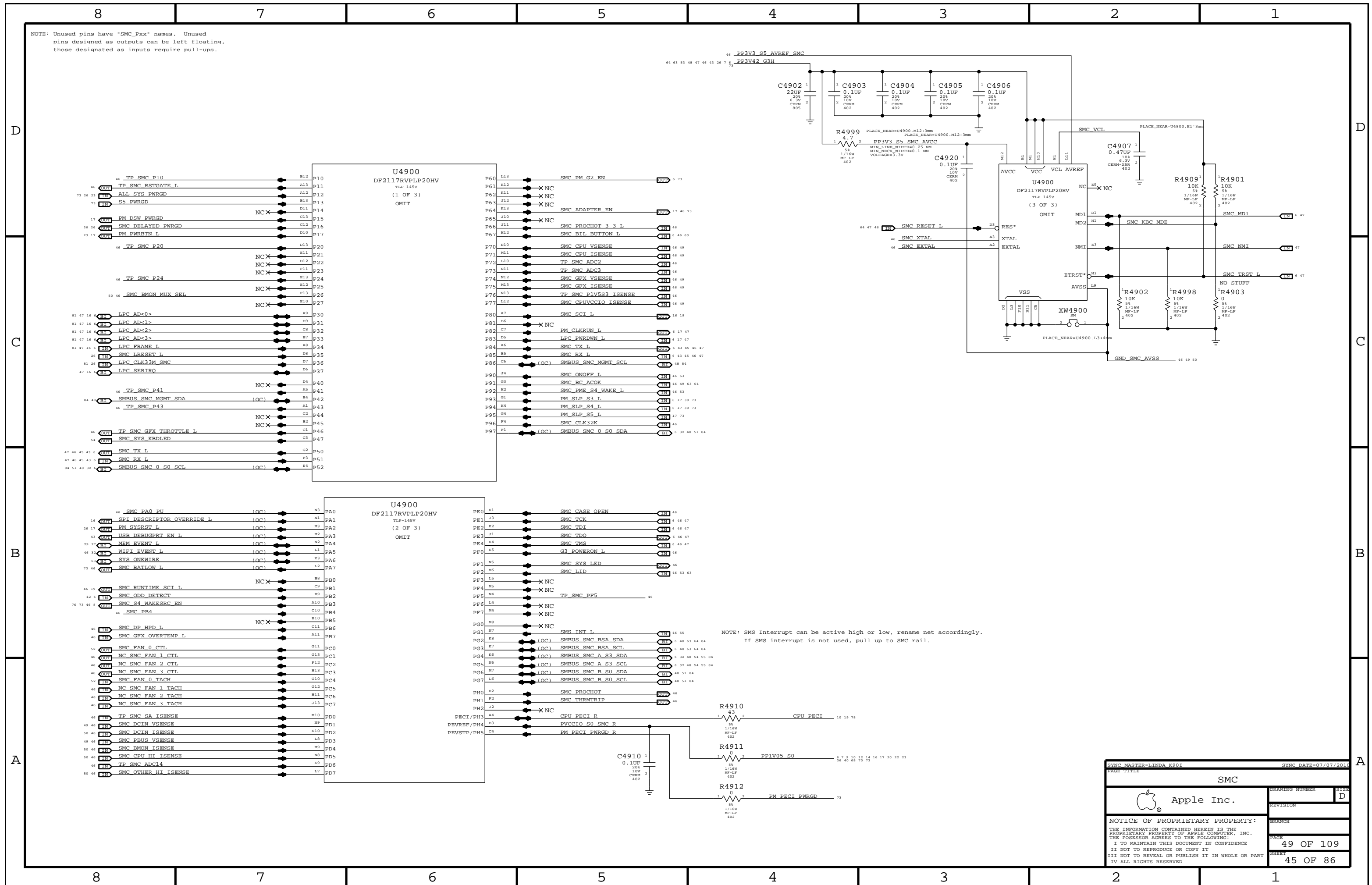
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- SYNC DATE=05/15/2010
- PAGE TITLE: Front Flex Support
- DRAWING NUMBER: D
- REVISION: I
- BRANCH: PAGE 48 OF 109
- SHEET: 44 OF 86

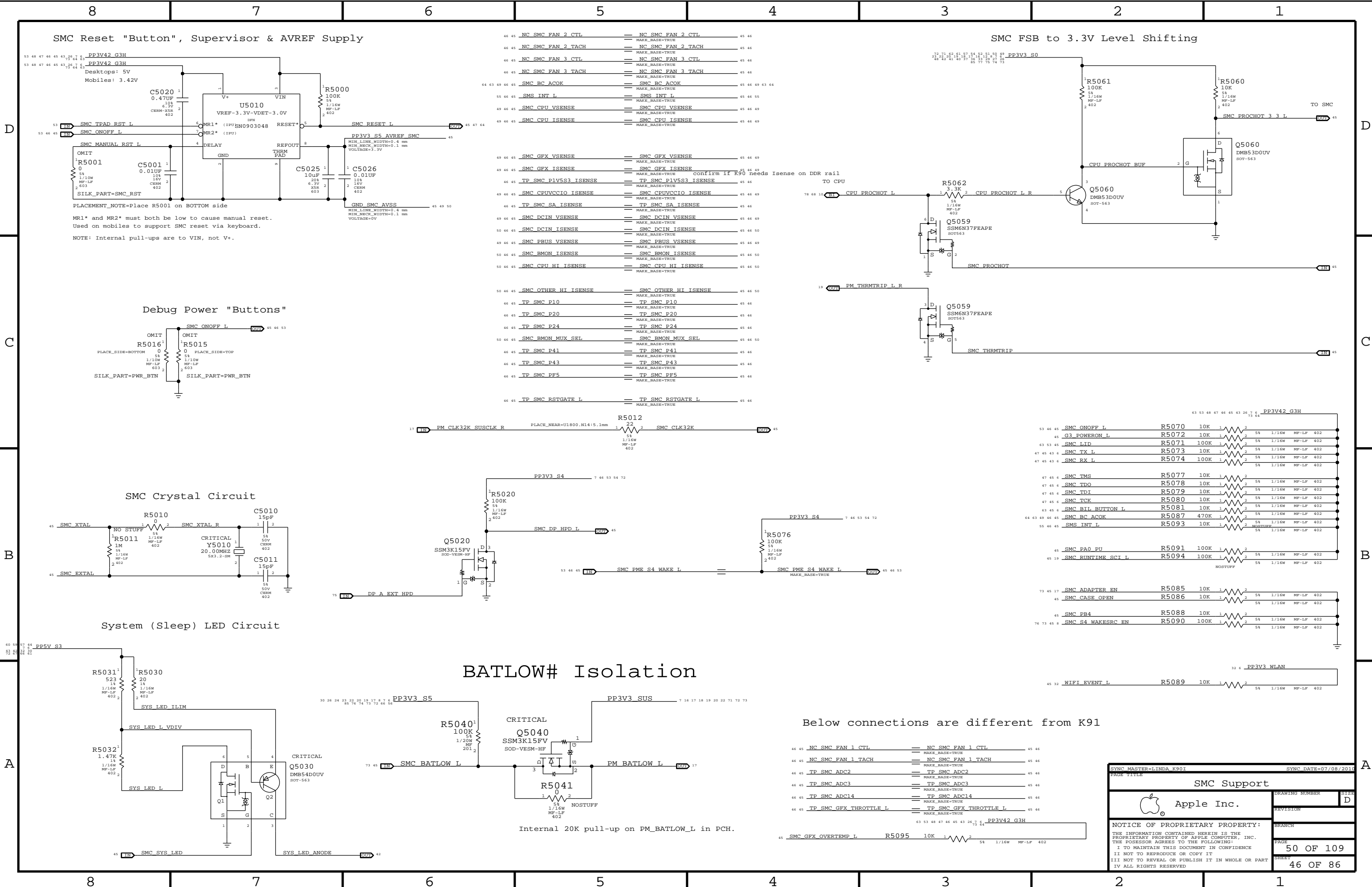
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SYNC DATE=07/08/2010

SMC Support

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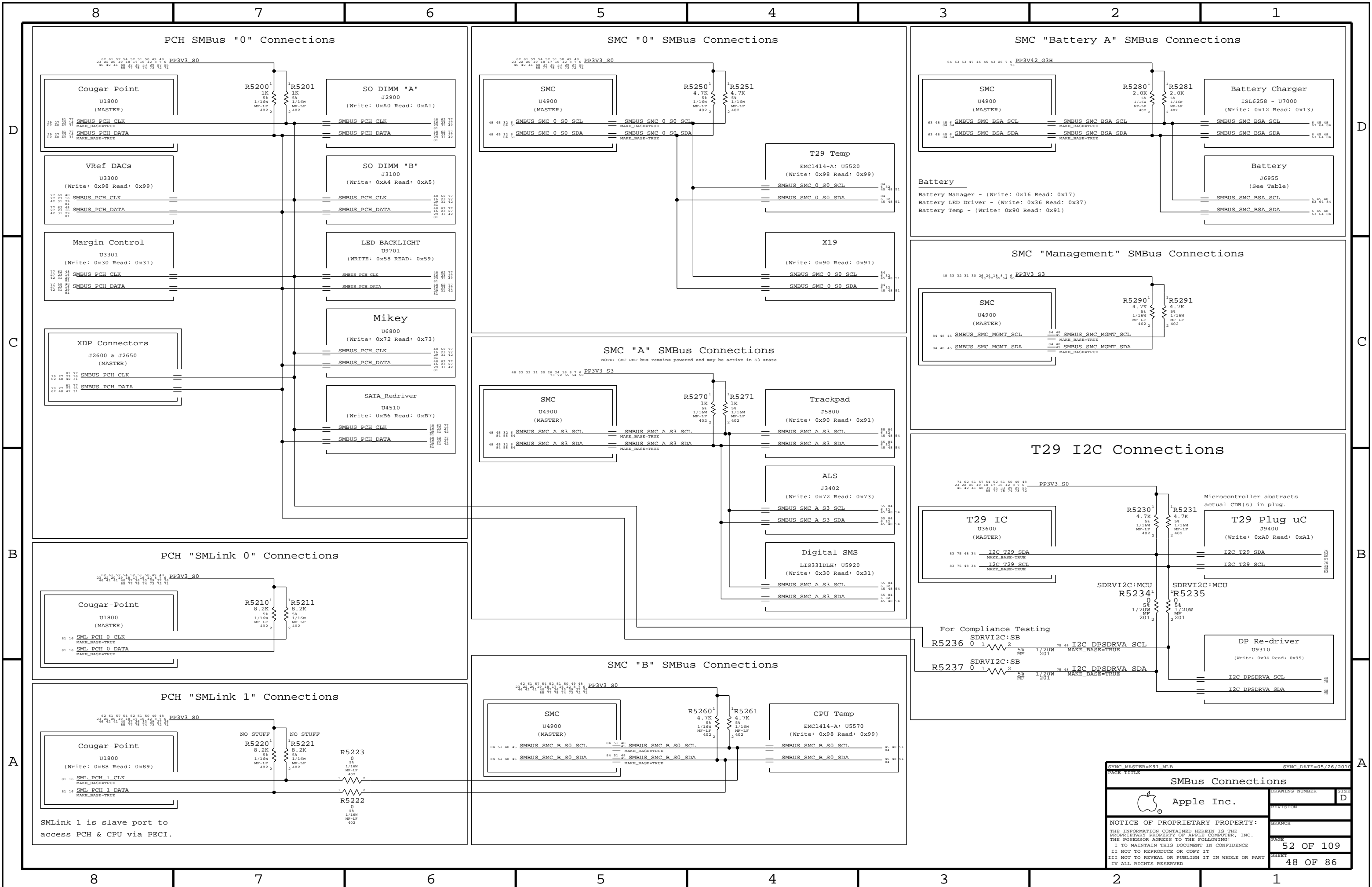
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SIZE

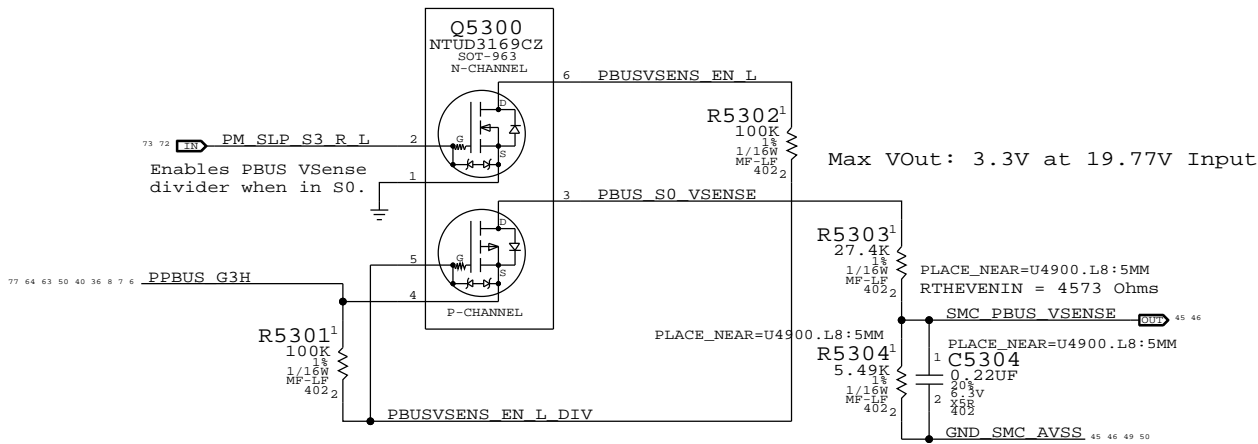
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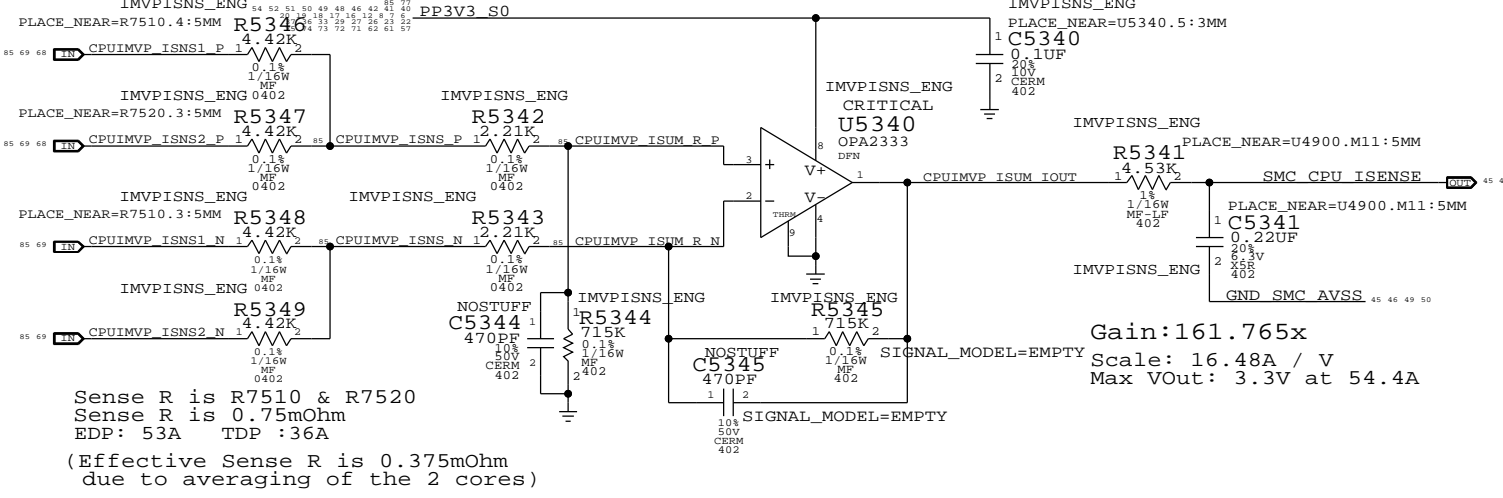
46 OF 86



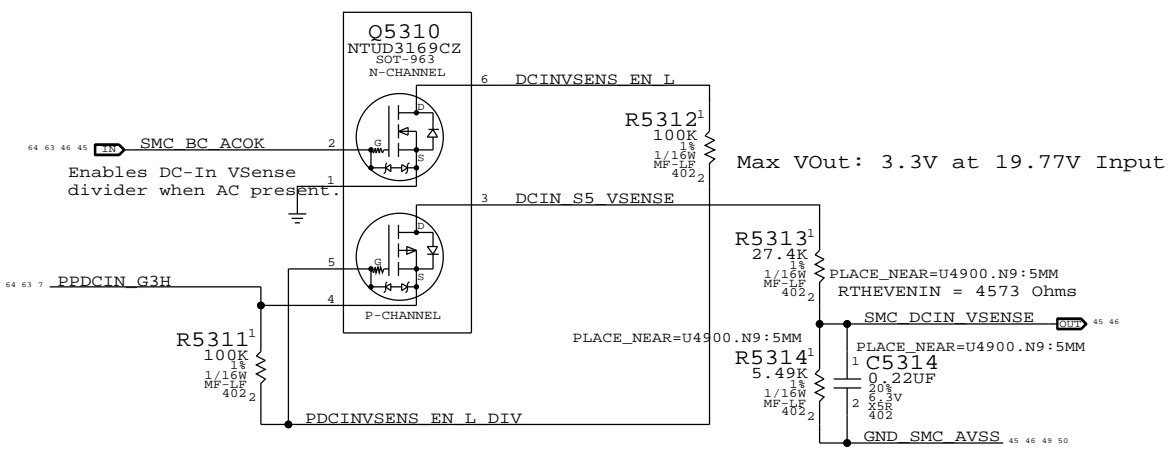
PBUS Voltage Sense Enable & Filter



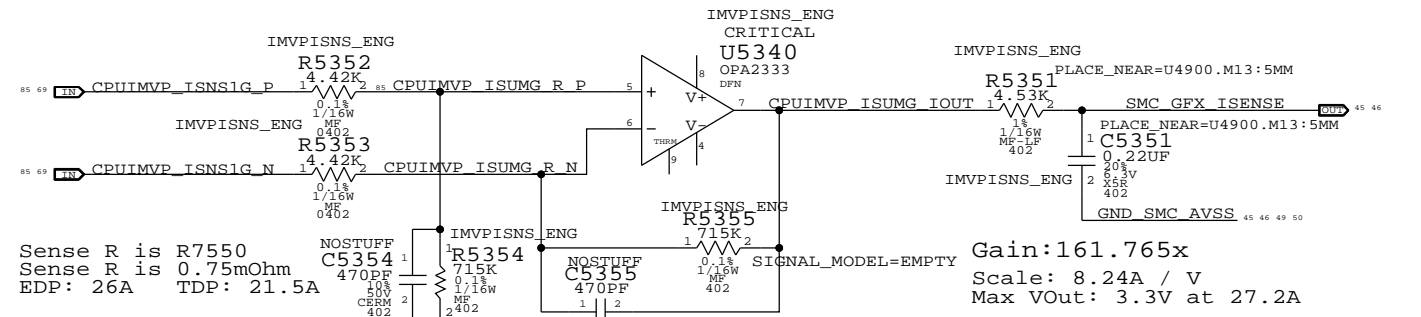
CPU VCore Load Side Current Sense / Filter



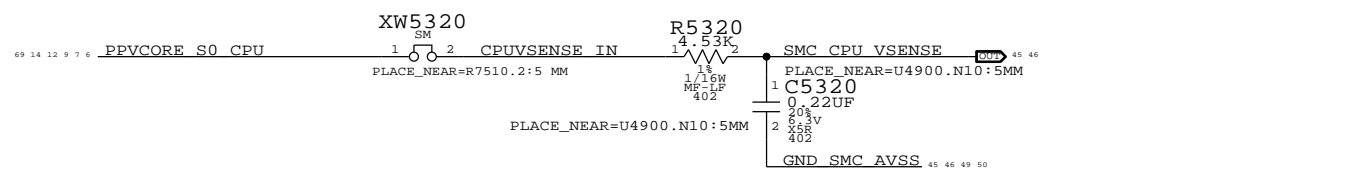
DC-In Voltage Sense Enable & Filter



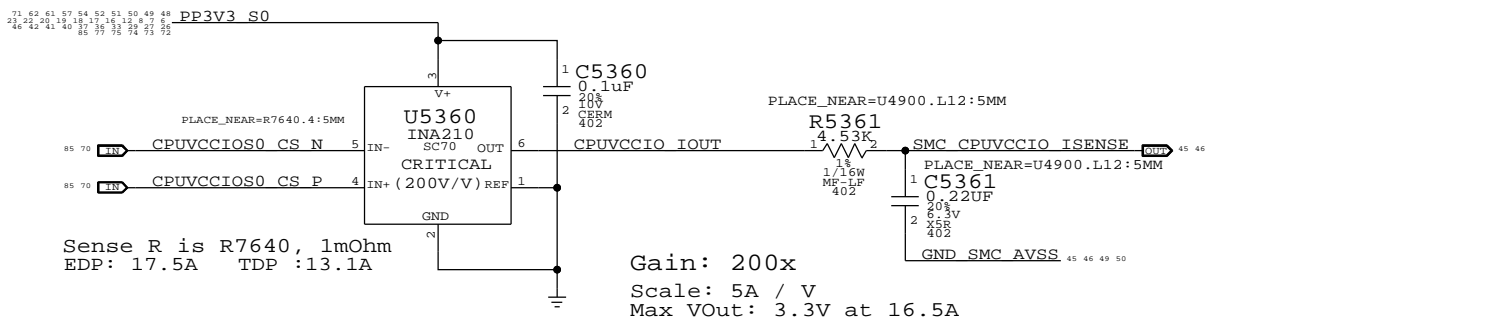
GFX/IG VCore Load Side Current Sense / Filter



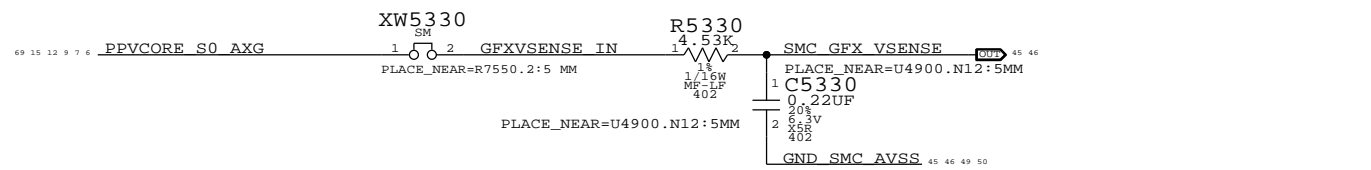
CPU Vcore Voltage Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



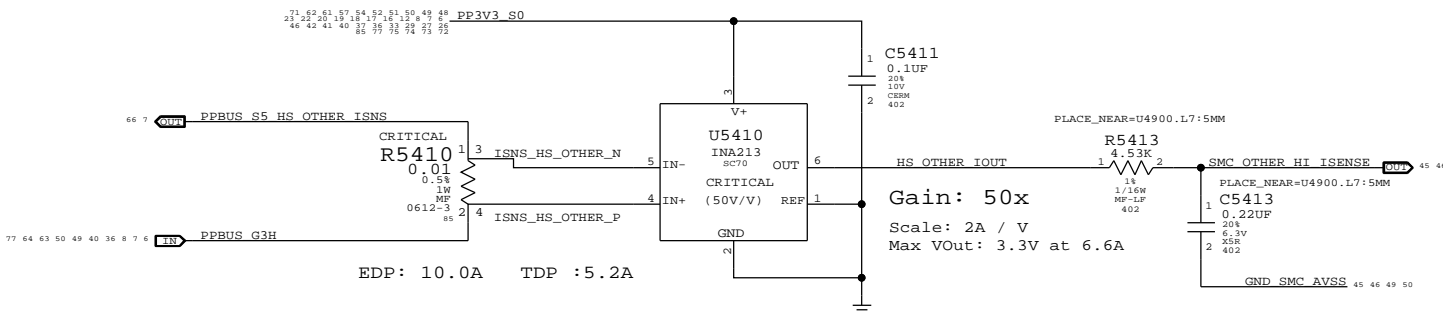
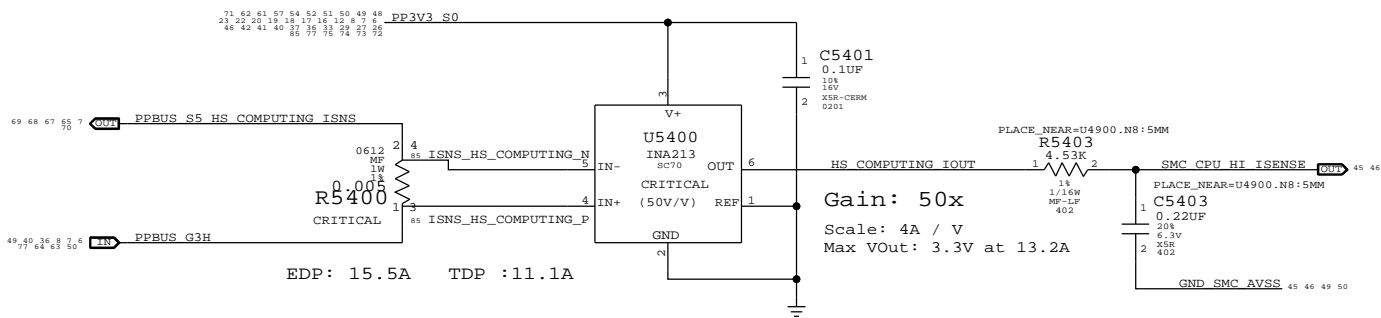
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Voltage & Load Side Current Sensing		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	D
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D

D

COMPUTING High Side Current Sense / Filter

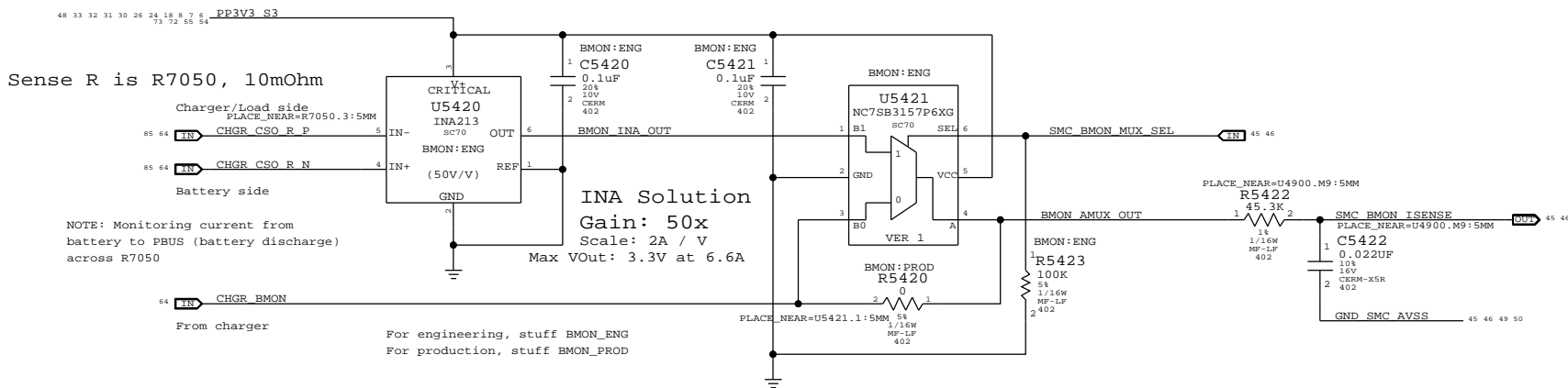
OTHER High Side Current Sense / Filter



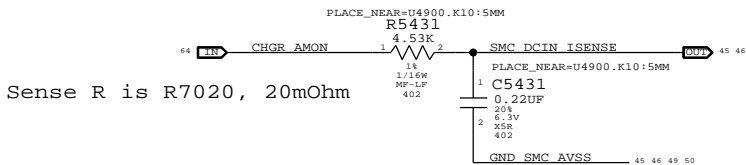
C

C

CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter



DC-IN (AMON) Current Sense Filter



DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

A

A

SYNC MASTER=LINDA K901		SYNC DATE=10/22/2010	
PAGE TITLE		High Side Current Sensing	
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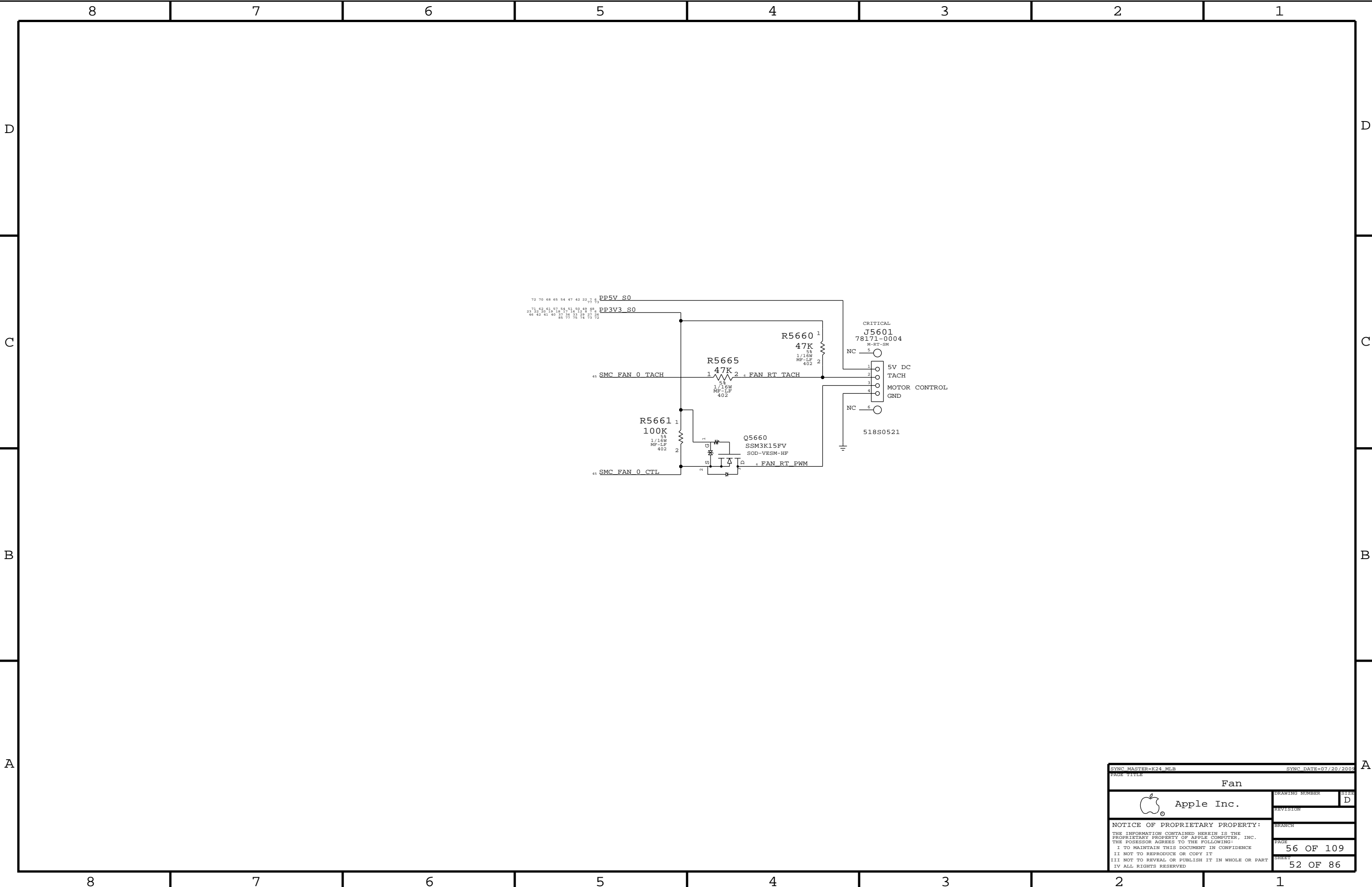



B



D

A



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Fan			
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.

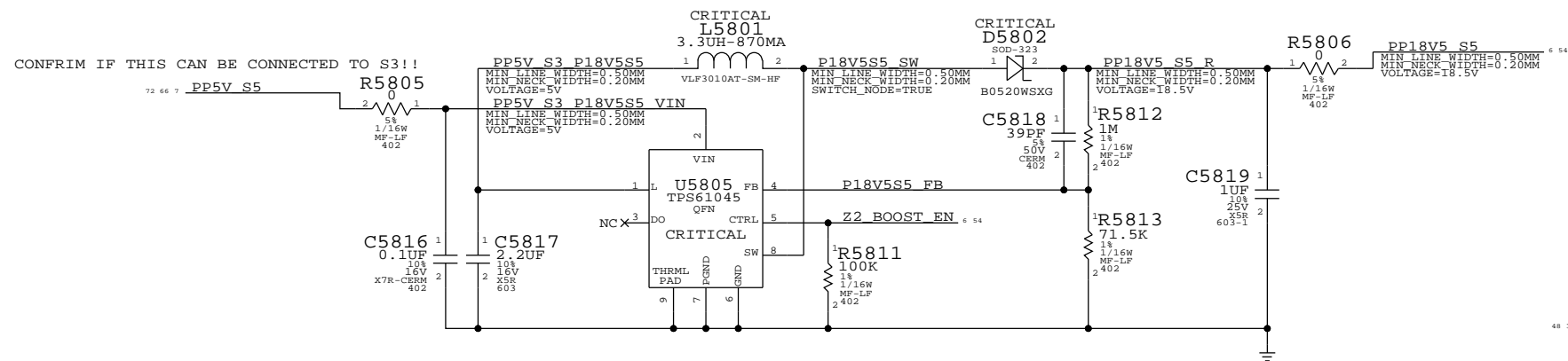
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		PAGE	57 OF 109
		SHEET	53 OF 86

TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V


```
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED
```



CRITICAL
J5800
55560-0228

M-ST-SM

PP3V3 S4

PP18V5 S5

Z2 CS L

Z2 DEBUG3

Z2 MOSI

Z2 MISO

Z2 SCLK

Z2 BOOST EN

Z2 HOST INTN

P3V3 S3 TPAD

Z2 CLKIN

N0 STUFF
R5800

S3

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VIA_PEN=3_V

516S0689

Z2 KEY ACT L

Z2 RESET

PSOC F_CS_L

PICKB_L

PSOC MISO

PSOC MOSI

PSOC_SCLK

SMBUS_SMC_A_S3_SDA

SMBUS_SMC_A_S3_SCL

72 70 68 65 52 47 42 22 73

PP5V3 S0

BYPASS=U5850.1:2:2 MM

72 71 62 61 57 52 51 50 49 48
23 22 20 19 18 17 16 15 8 7 6
46 42 41 40 37 36 33 29 27 25
85 77 76 74 73

PP3V3 S0

R5853¹
470K
5%
1/16W
MF-LF
402-2

KB_BL
C5850
10UF
10V
X5R
402-1

45 **SMC_SYS_KBDLED**

Keyboard backlight, SMC will
nd read SMC_SYS_KBDLED:
yboard backlight present
eyboard backlight not present
ys stuffed, R5854 only
hen KB BL flex connected.

KB_BL
R5854
4.7K
5%
1/16W
MF-LF
402-2

NO STUFF
R5852¹
10K
5%
1/16W
MF-LF
402-2

CRITICAL
KB_BL
L5850
10UH-0.58A-0.35OHM

1 2 KBDLED_SW
109BAS-SM
MIN LINE WIDTH=0.3 MM
MIN NECK WIDTH=0.25 MM
SWITCH_NODE=TRUE

CRITICAL SW
VIN
LED
CTRL
5

KB_BL
U5850
LT3491
DPH

6

KB_BL
R5855
10
1%
1/16W
MF-LF
402-2

KBDLED ANODE
MIN LINE WIDTH=0.25 MM
MIN NECK WIDTH=0.25 MM

KB_BL
KBDLED CAP
MIN LINE WIDTH=0.25 MM
MIN NECK WIDTH=0.25 MM

4

KB_BL
C5855
10UF
35V
2
X5R
403

(SMC KBDLED PRESENT I)

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 not grounded when KB BL flex connected.

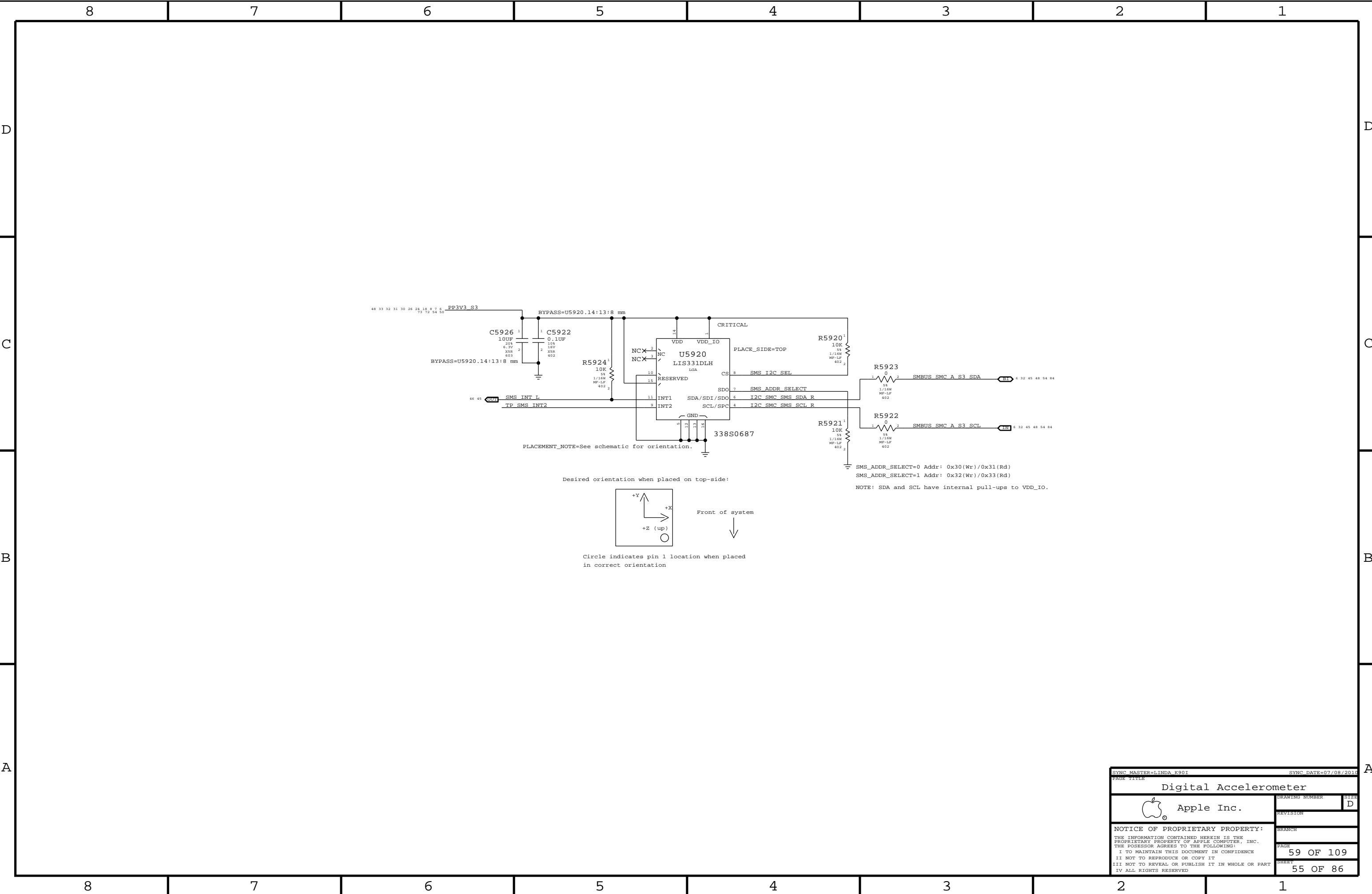
CRITICAL


KB BL
J5815
FF18-4A-R11AD-B-3H
FF18-04

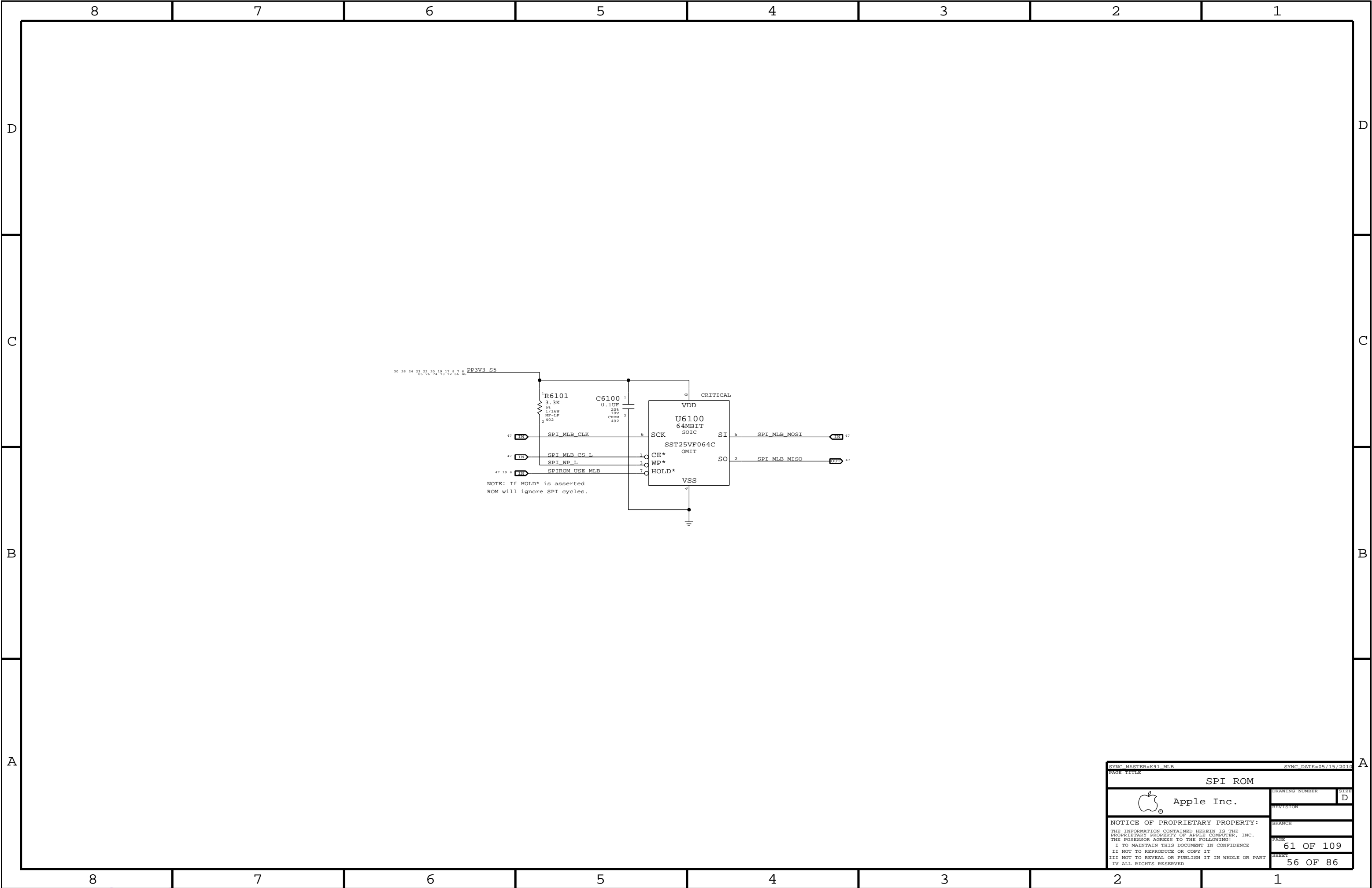
SMC KDBLED PRESENT L

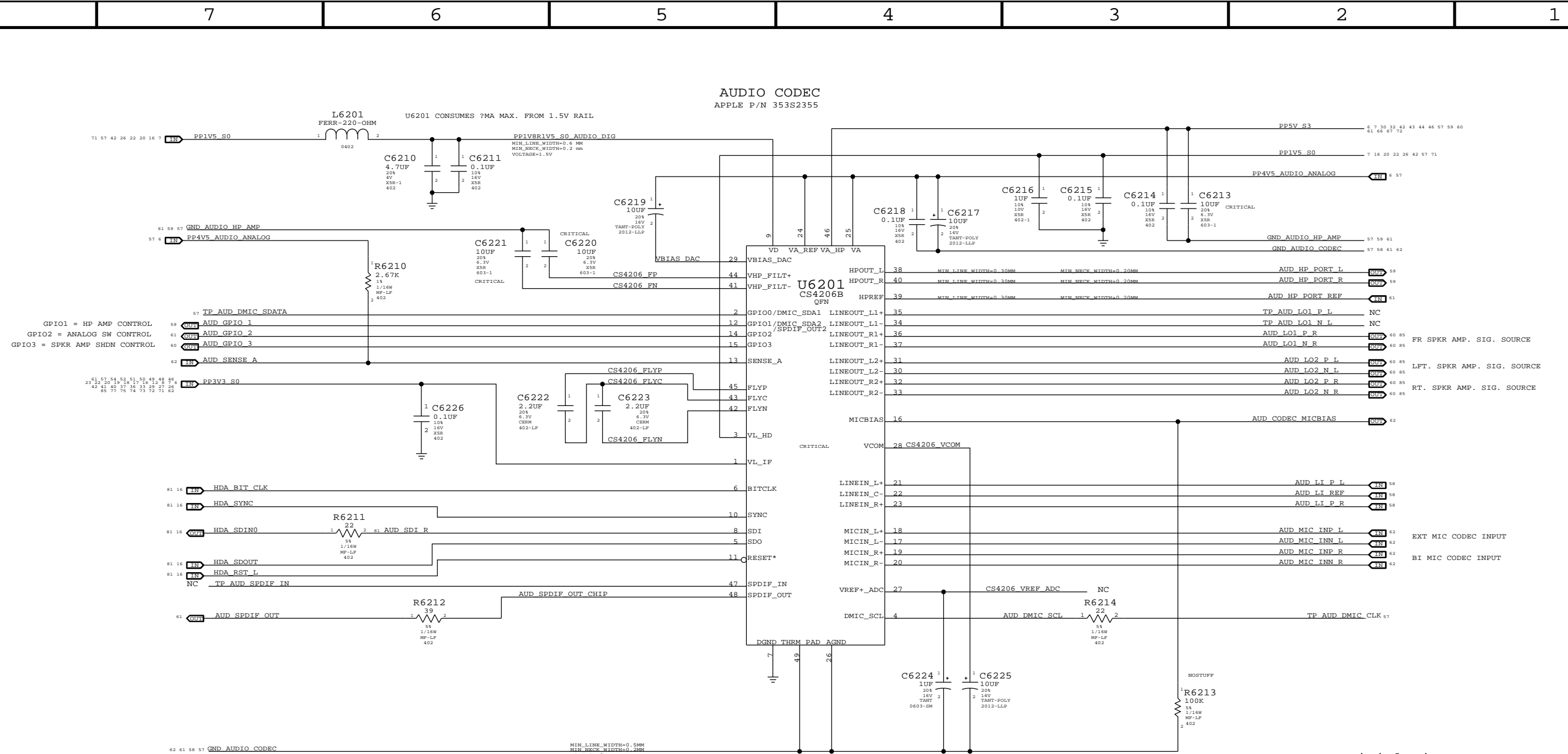
J5815 pin 1 is grounded
on keyboard backlight flex

518S0691

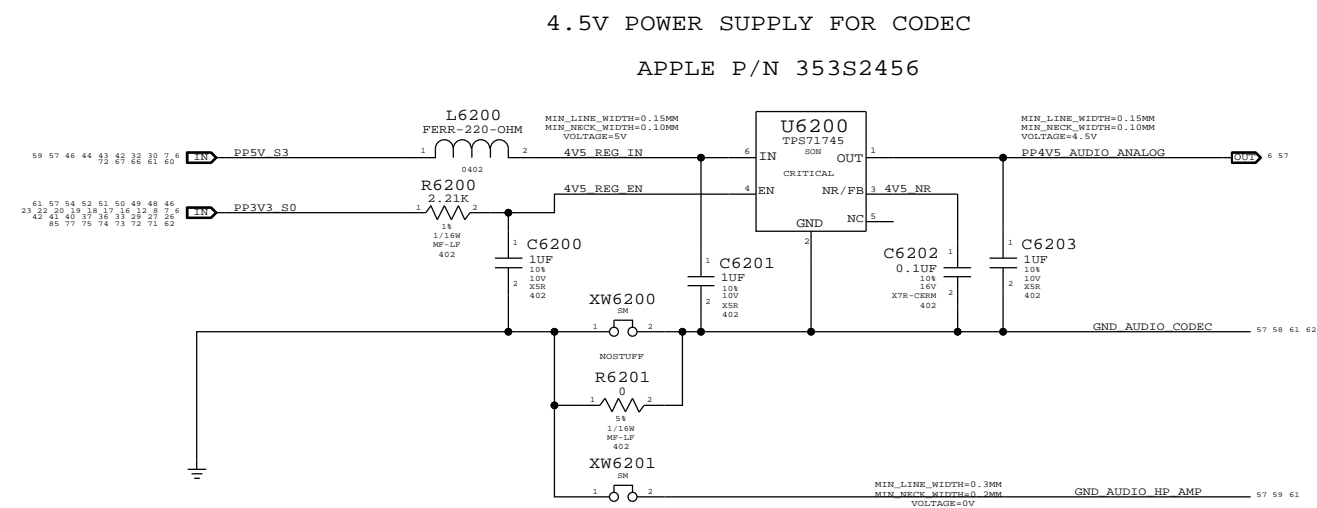


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		PAGE	59 OF 109
		SHEET	55 OF 86






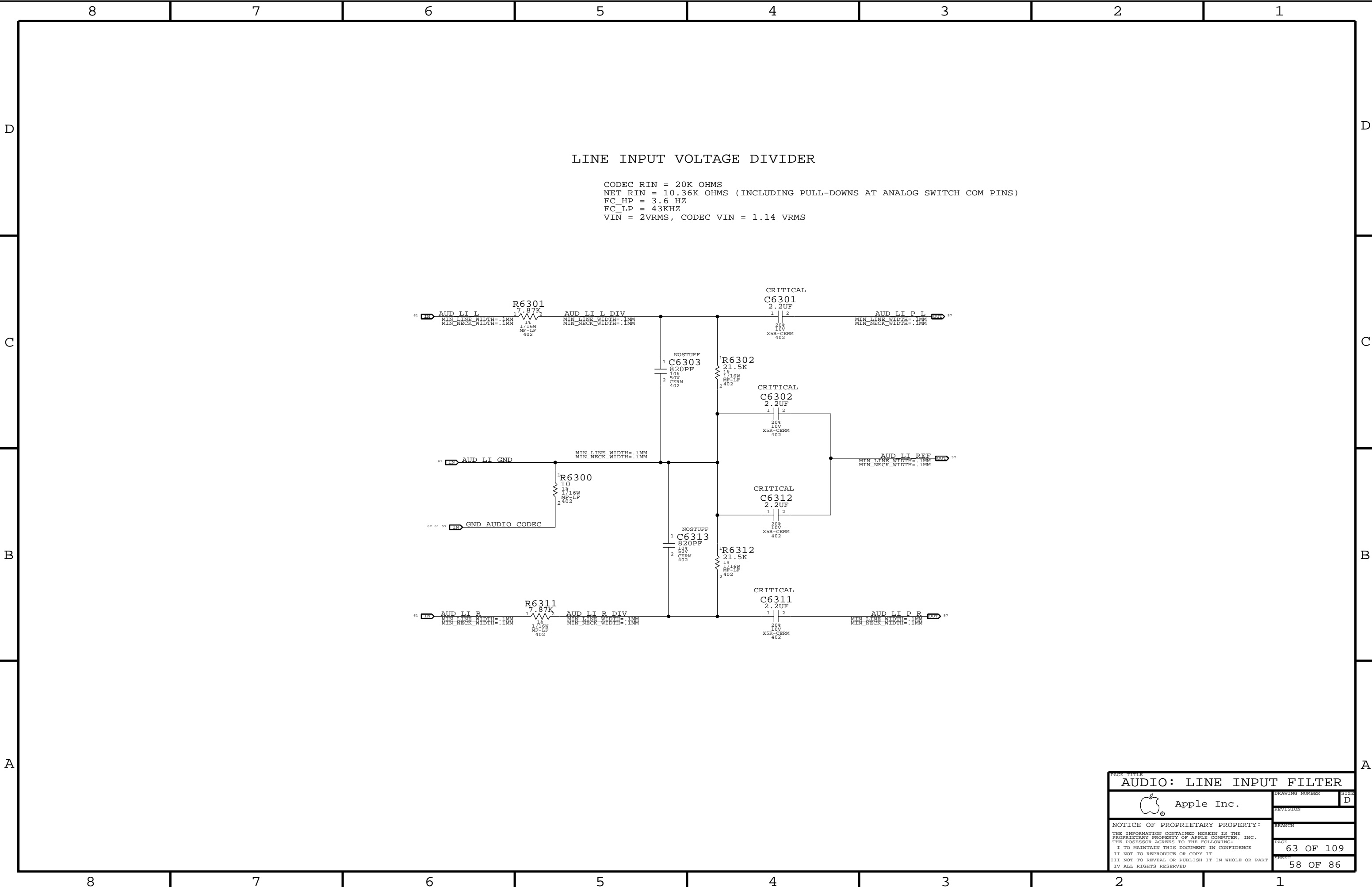
Digital Mic

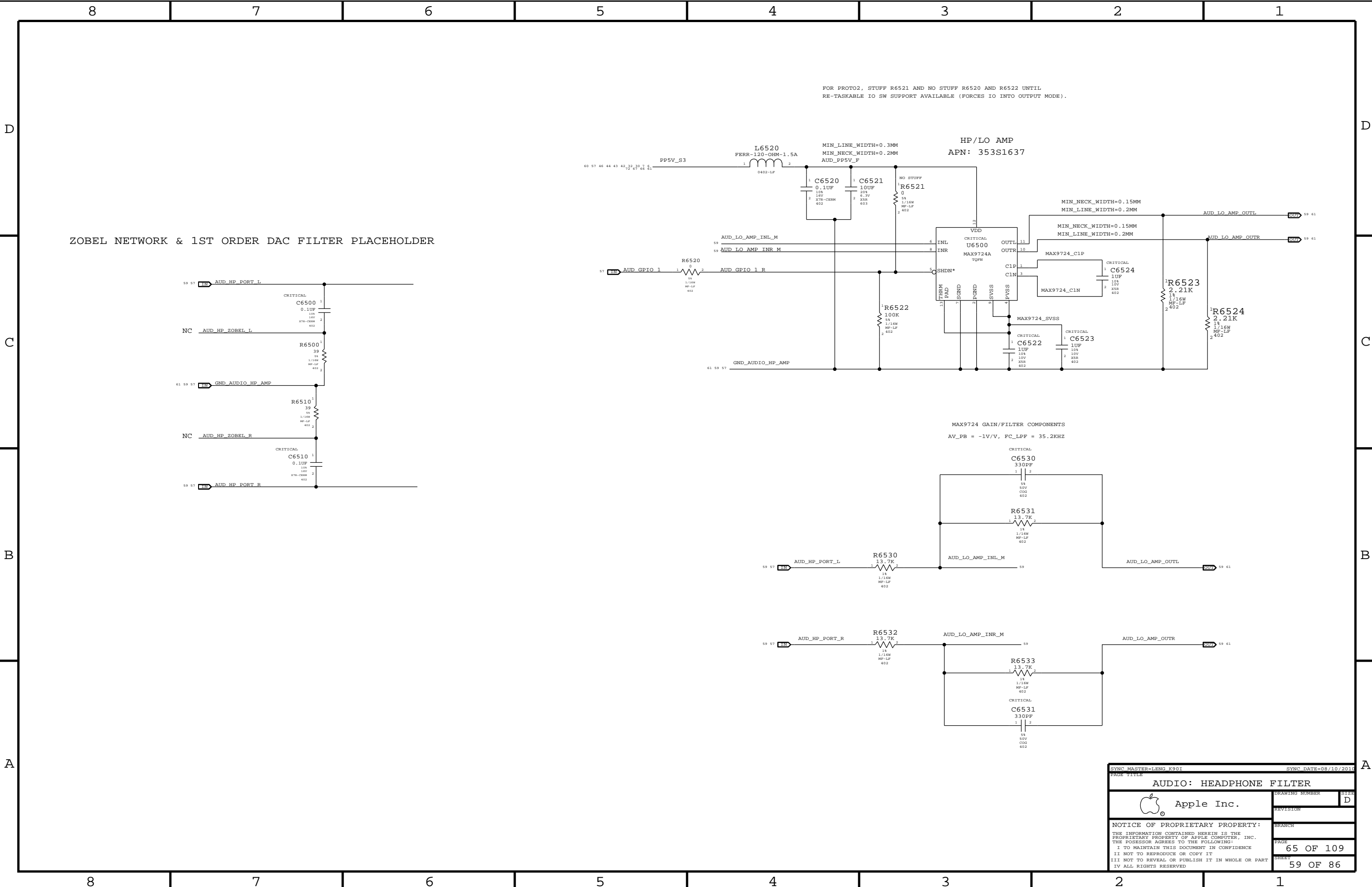


NOTES ON CODEC I/O

```
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
```

SYMC MASTER=LENG E901		SYMC DATE=08/10/2010	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
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		SIZE	
		REVISION	
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		SHEET 57 OF 86	






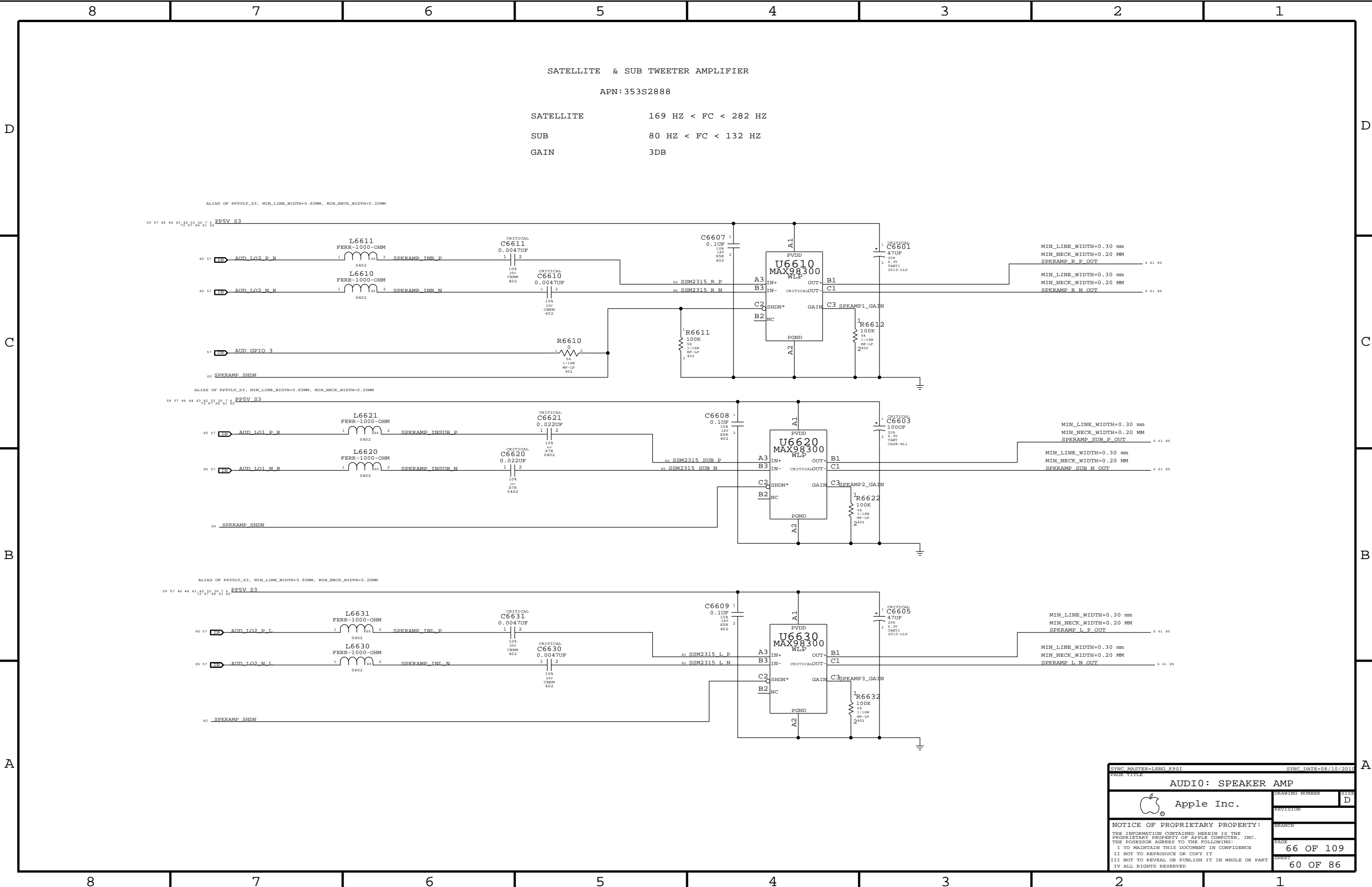
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ

SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
 Apple Inc.	DRAWING NUMBER		SIZE
			D
REVISION			
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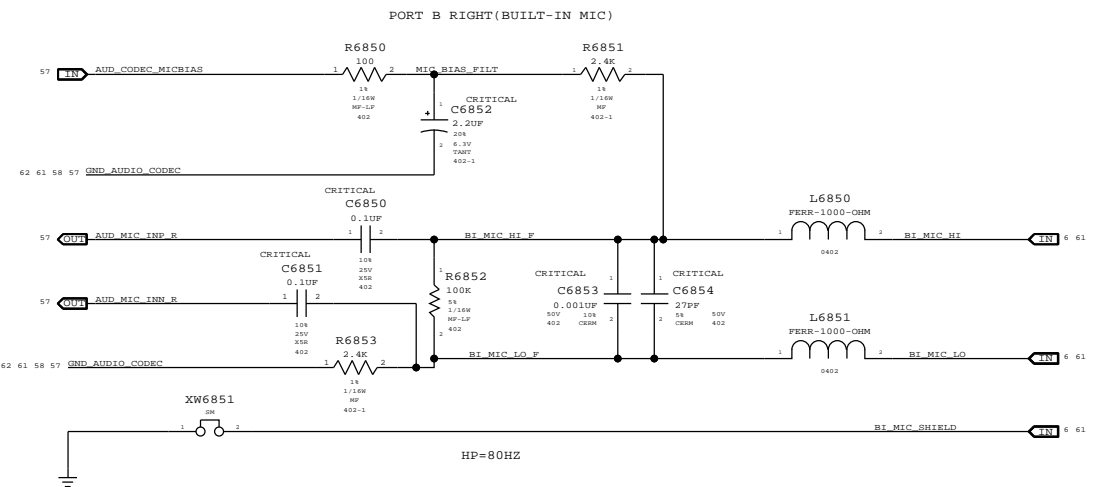
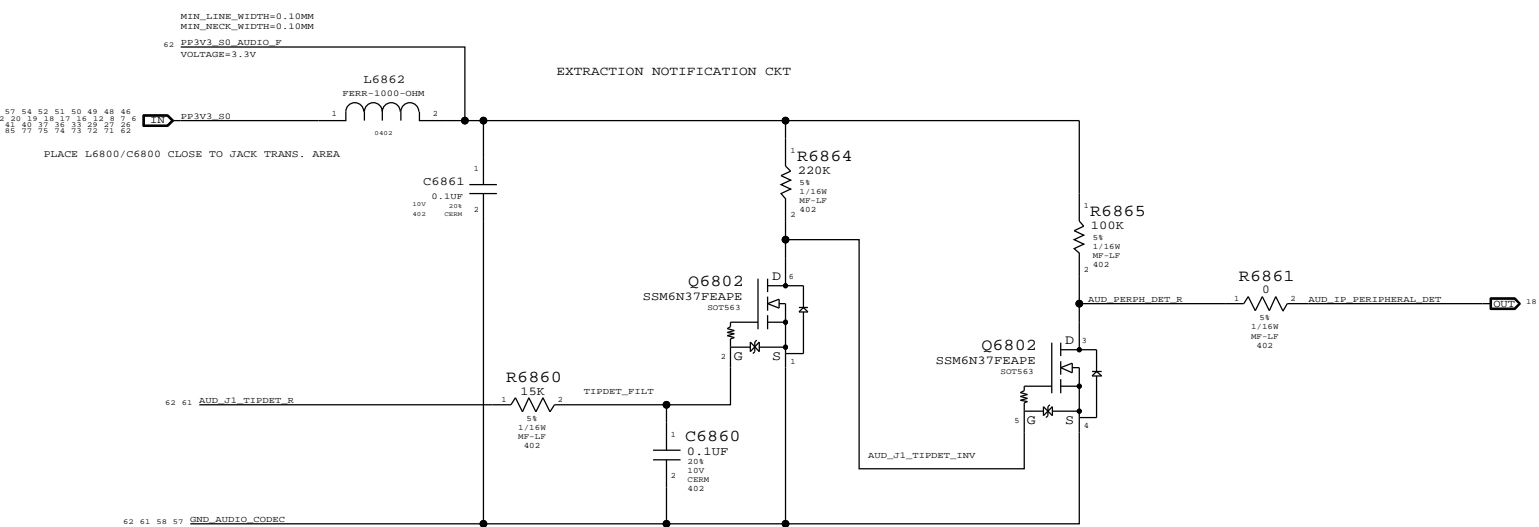


SYNC MASTER=LENG K901		SYNC DATE=08/10/2010	
PAGE TITLE			
AUDIO0: SPEAKER AMP			
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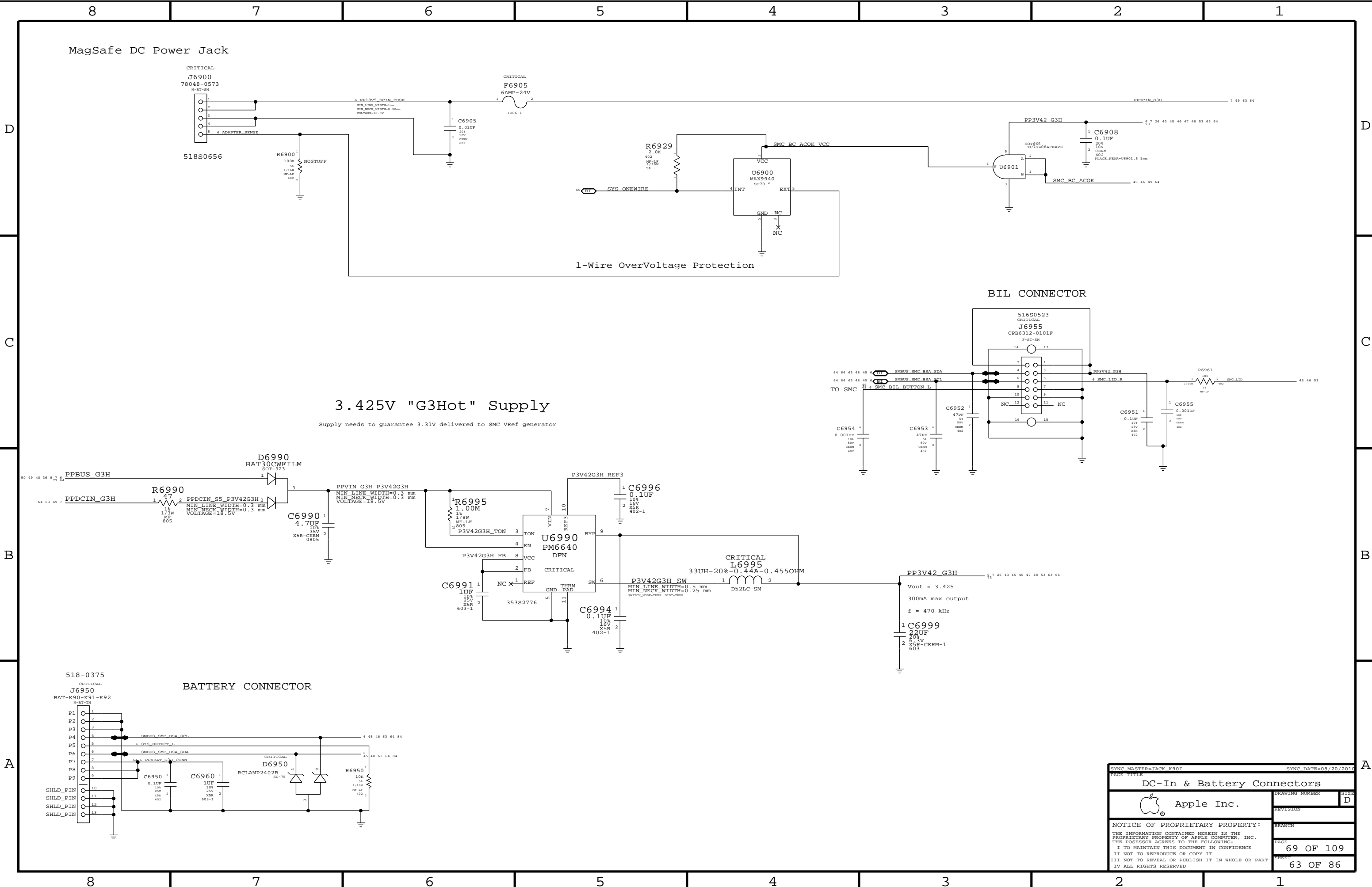


CODEC INPUT SIGNAL PATHS				
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES) PORT B DETECT

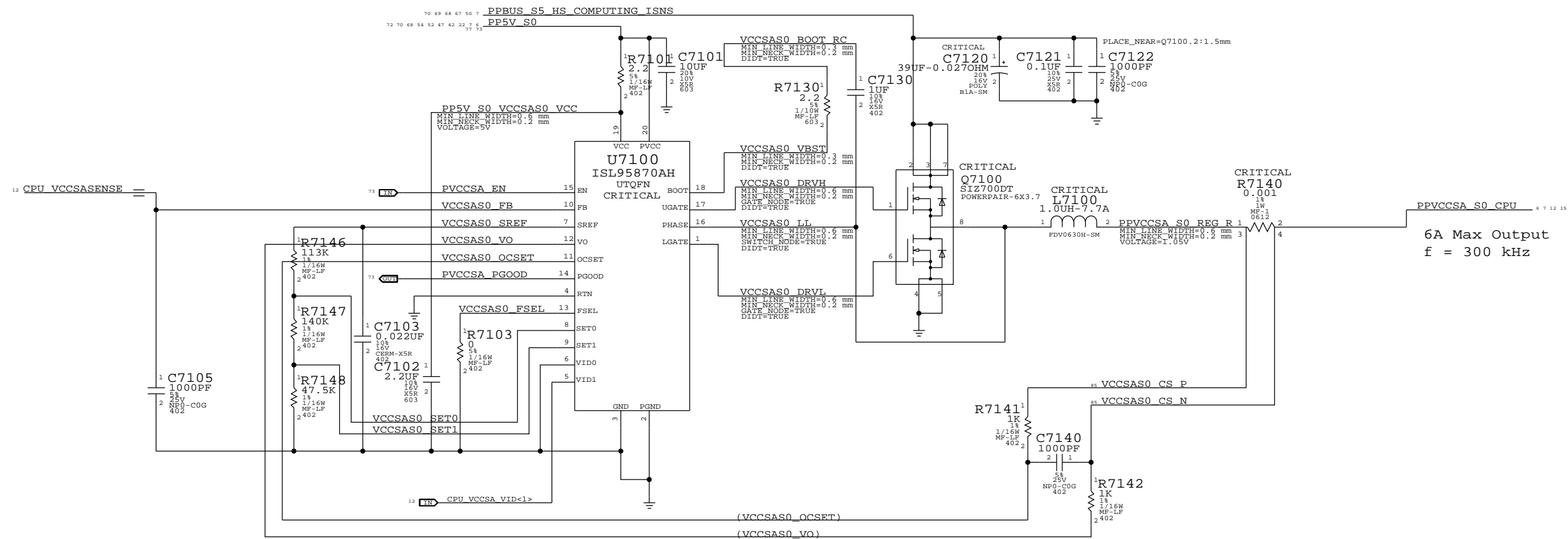



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System Agent Power Supply



SYNC MASTER=JACK K901		SYNC DATE=08/19/2010	
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System Agent Supply			
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5V_S3 / 3.3V_S5 POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$

$V_{OUT} = (2 * R_C / R_D) + 2$

MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

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5V_S3 / 3.3V_S5 POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$

$V_{OUT} = (2 * R_C / R_D) + 2$

MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

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5V_S3 / 3.3V_S5 POWER SUPPLY

$V_{OUT} = (2 * R_A / R_B) + 2$

$V_{OUT} = (2 * R_C / R_D) + 2$

MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

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5V_S3 / 3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2

MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A

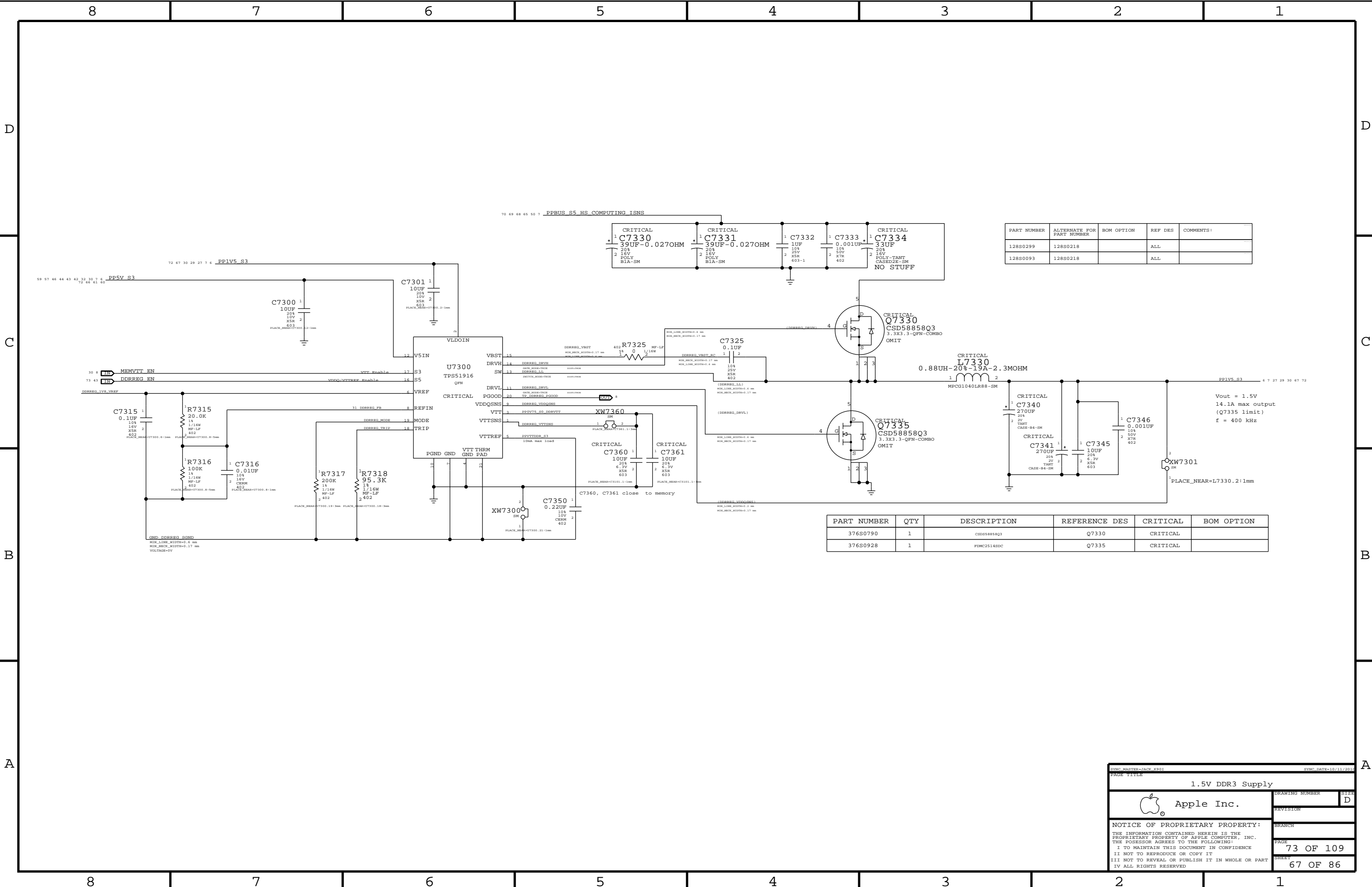
SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD58858Q3	Q7330	CRITICAL	
376S0928	1	FDMC25148DC	Q7335	CRITICAL	

Vout = 1.5V
14.1A max output
(Q7335 limit)
f = 400 kHz

SYMC PARTNERS-JACK K802

SYMC DATE=10/11/2016

1.5V DDR3 Supply

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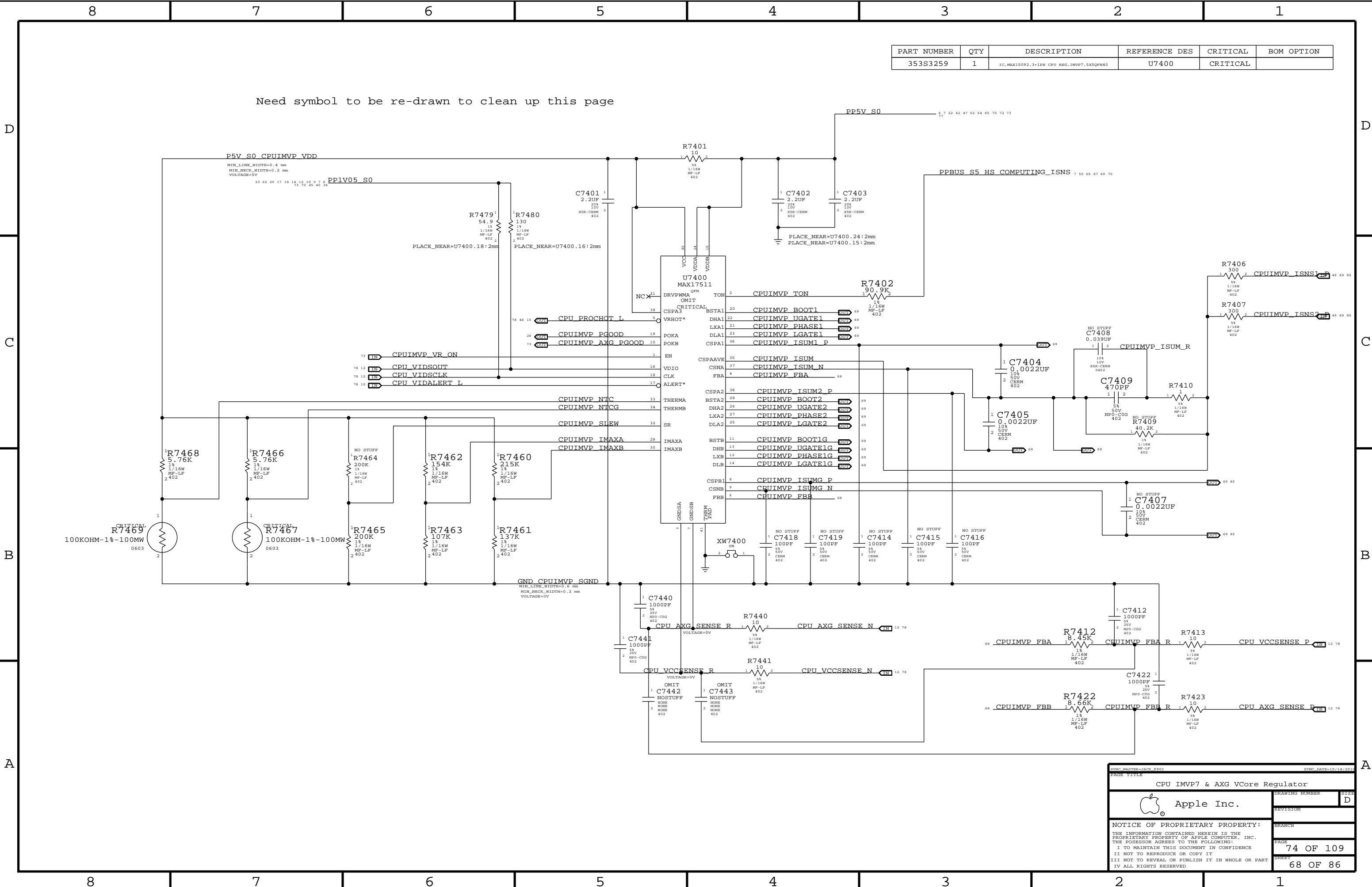
SHEET

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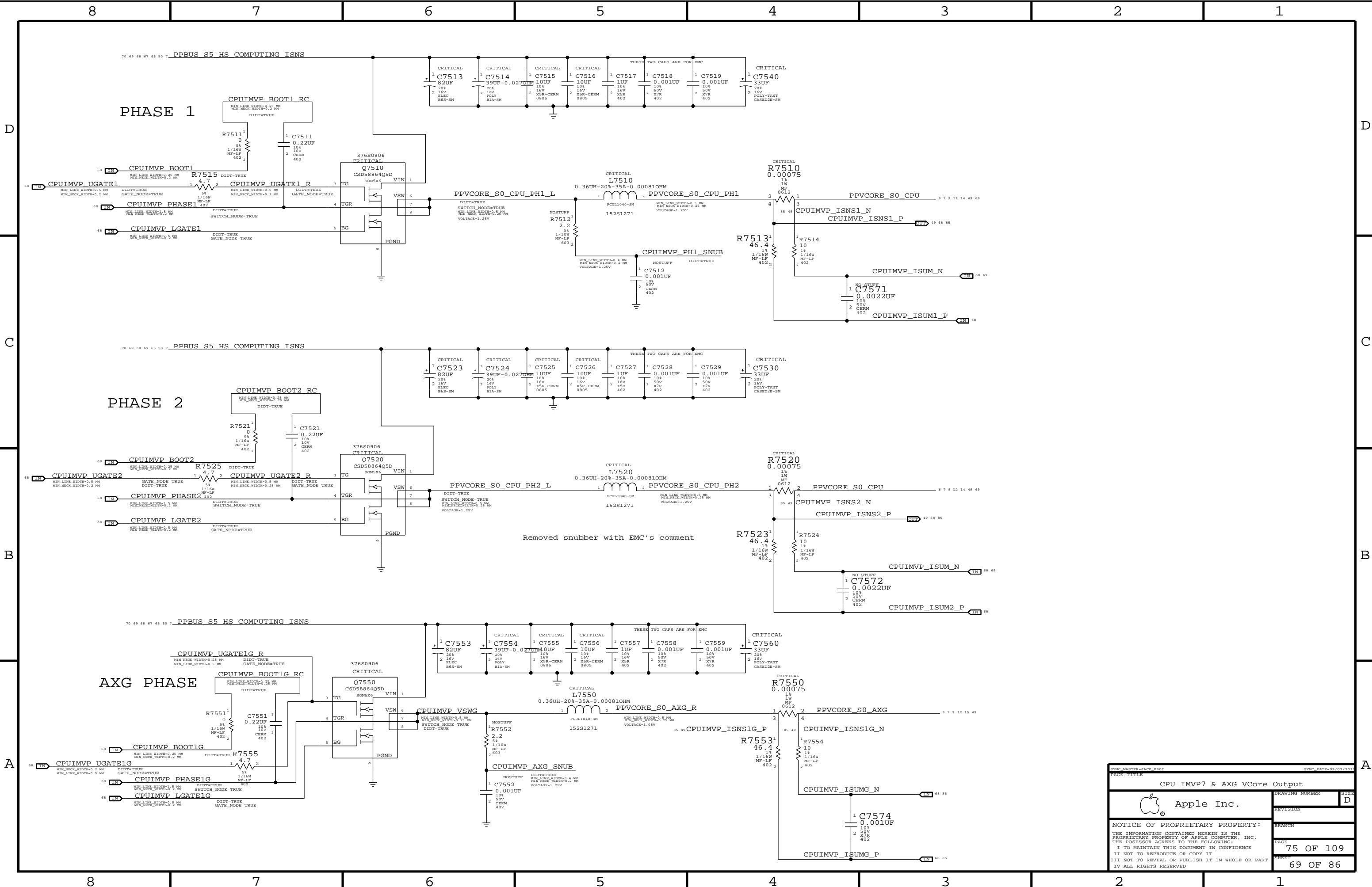
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
D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC_MAX15092,3+1PH CPU REG,1MVP7,5X5QFN40	U7400	CRITICAL	

PAGE TITLE		SYNCH DATE:10/14/2015	
CPU IMVP7 & AXG VCore Regulator		DRAWING NUMBER	SIZE
Apple Inc.		REVISION	D
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SYMC PART#-JACK_K902		SYMC DATE=09/03/2016	
PAGE TITLE			
CPU IMVP7 & AXG VCore Output		DRAWING NUMBER	SIZE
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D



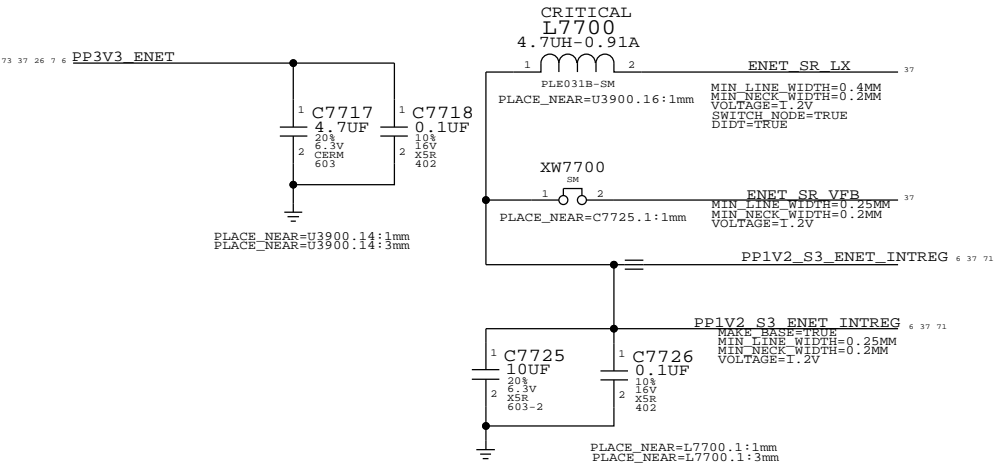
C

B

A

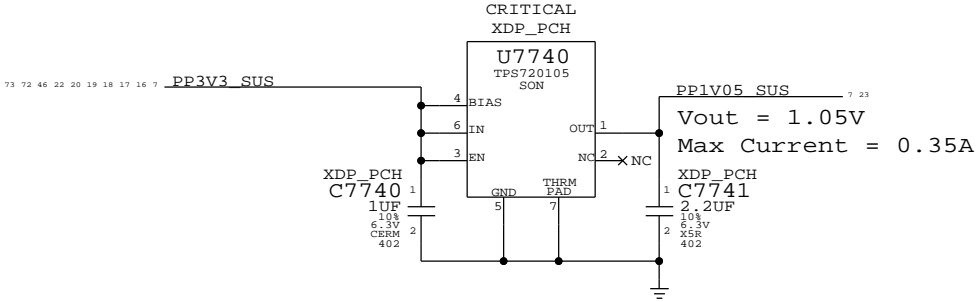
A

CAESAR IV 1.2V INT.VR CMPTS



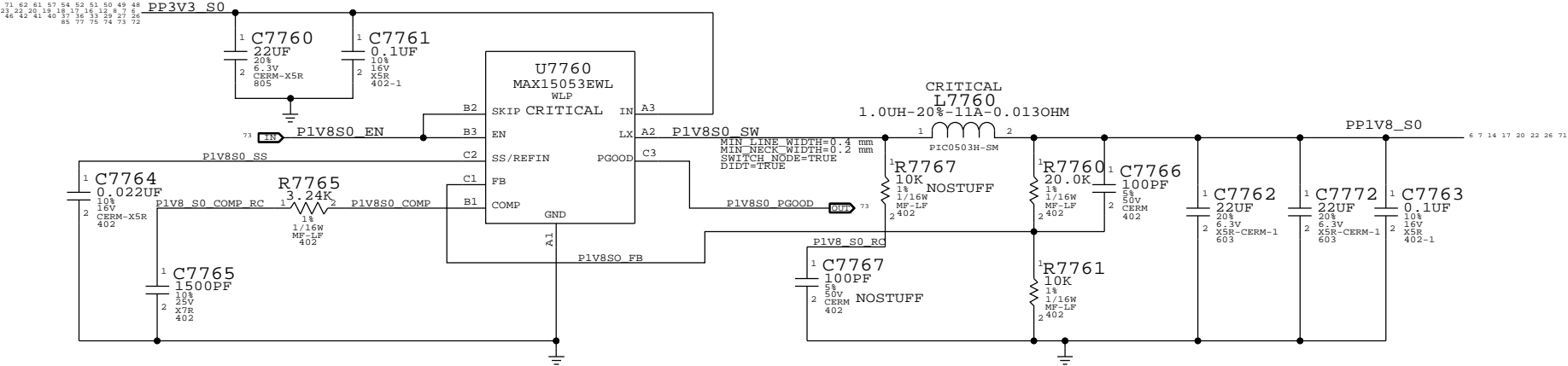
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



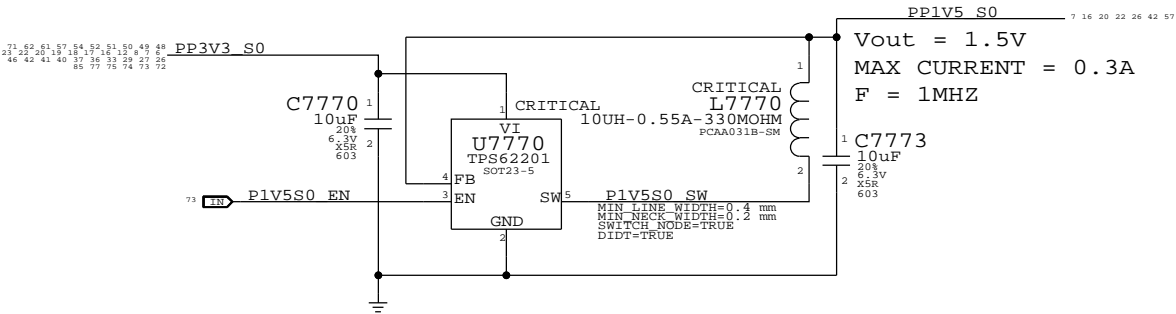
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



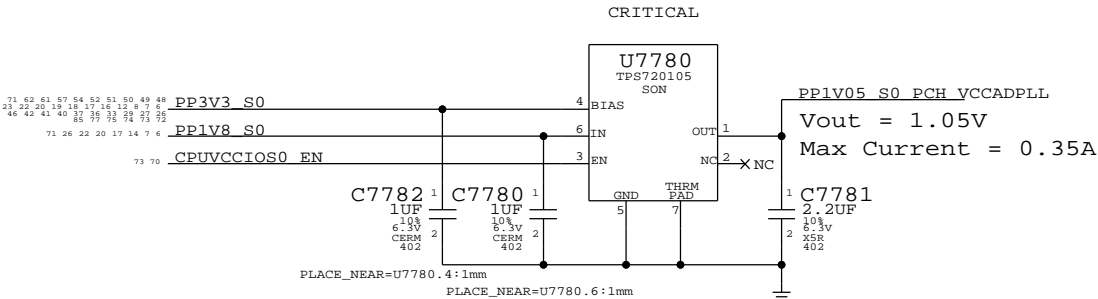
1.5V S0 Switcher

Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ

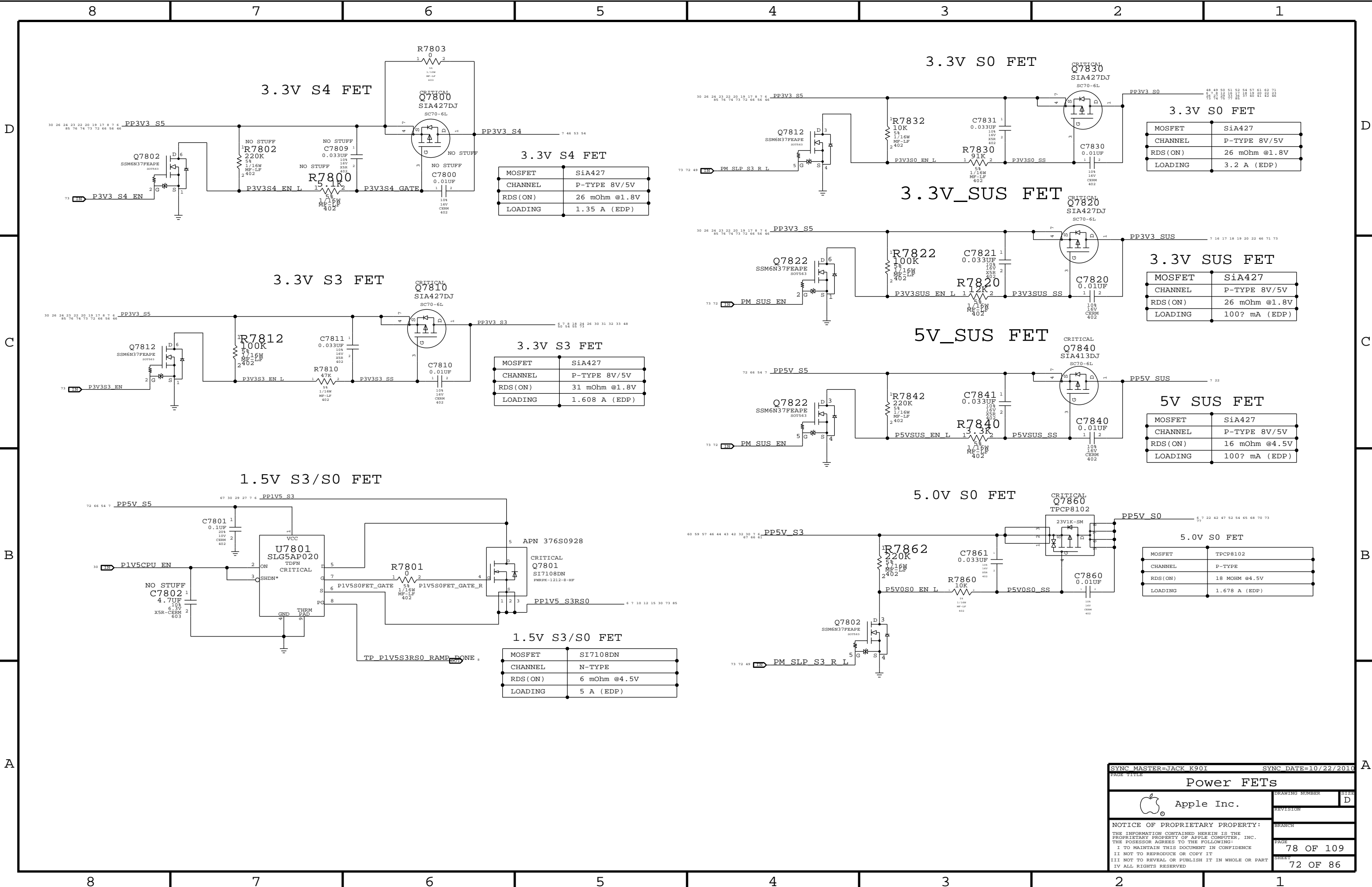


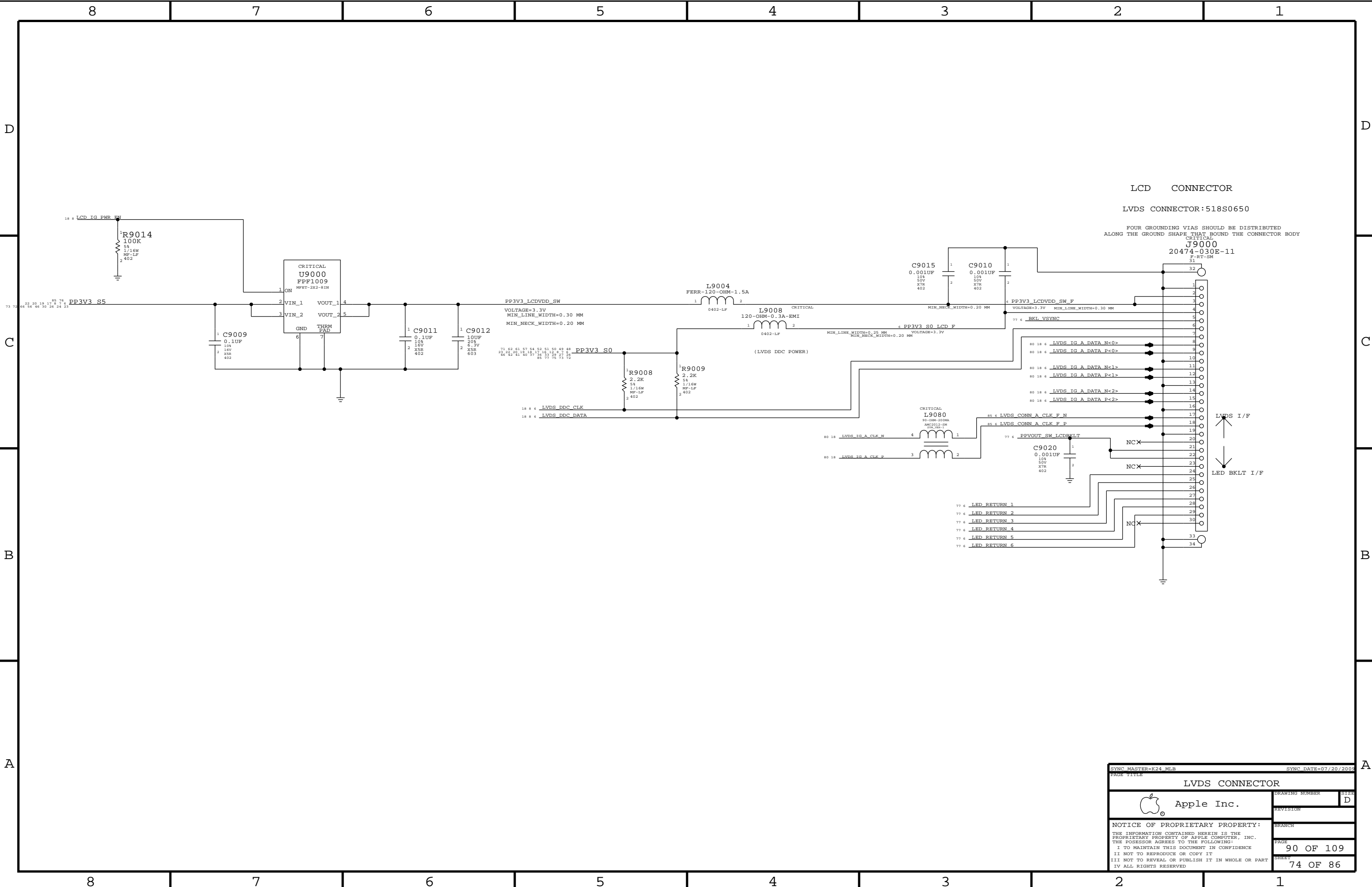
1.05V S0 LDO

Vout = 1.05V
Max Current = 0.35A



SYNC MASTER=JACK K901		SYNC DATE=08/19/2010	
PAGE TITLE		Misc Power Supplies	
Apple Inc.		DRAWING NUMBER	SIZE
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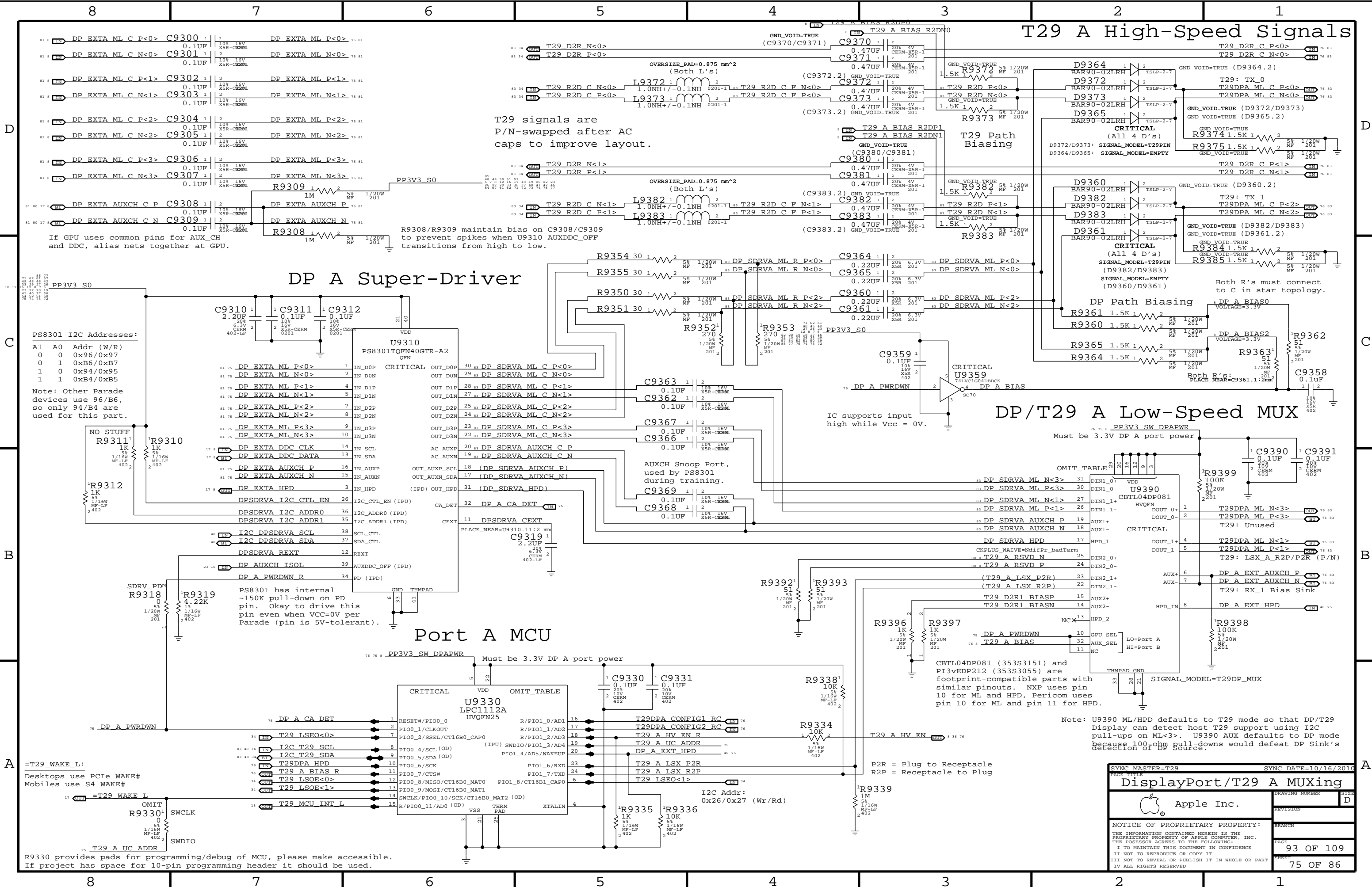
LCD CONNECTOR
LVDS CONNECTOR:518S0650

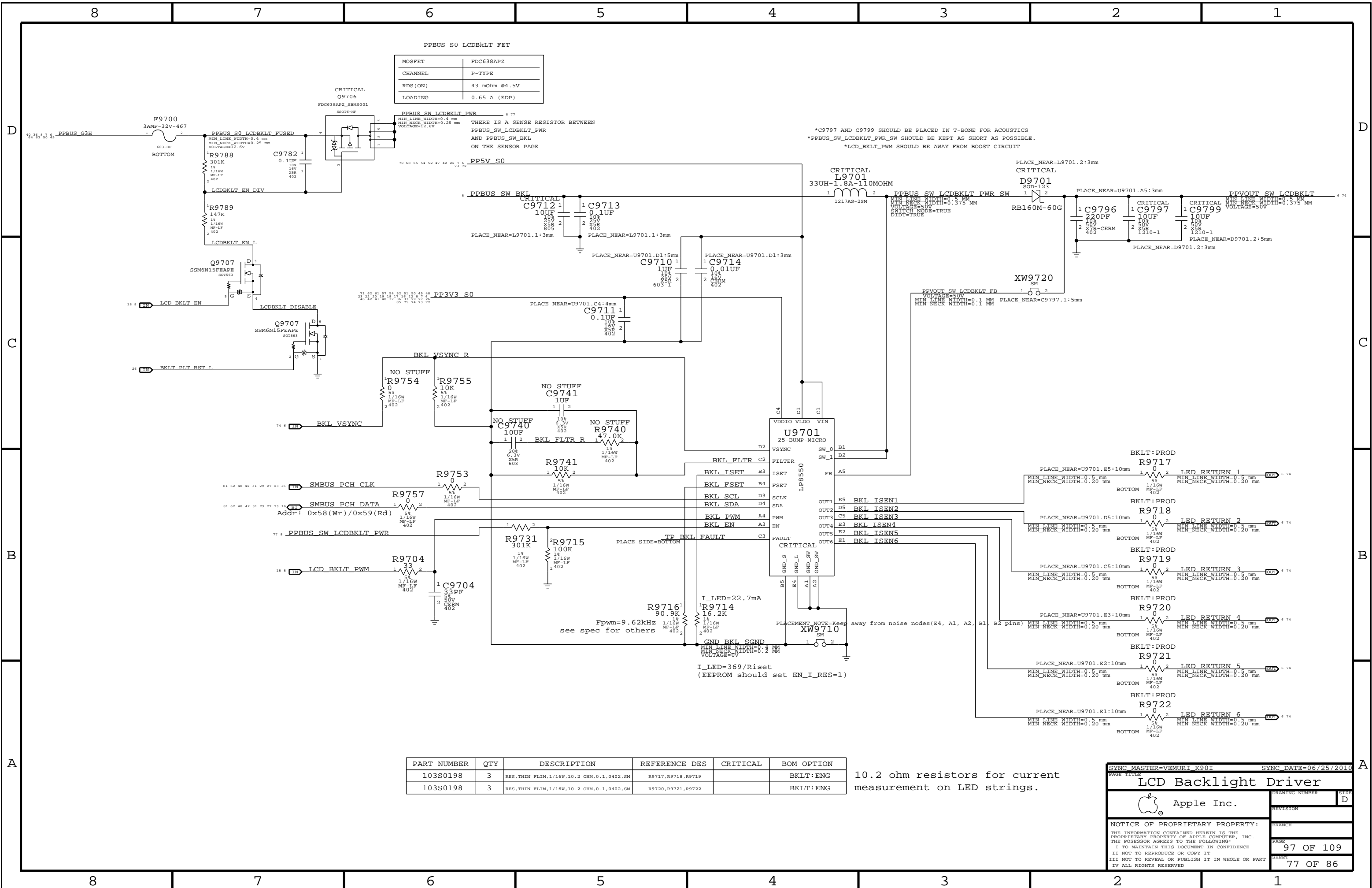
FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY

CRITICAL
J9000
20474-030E-11
F-RT-SM

LVDS I/F
LED BKLT I/F


SYNC MASTER=K24 MLB		SYNC DATE=07/20/2009	
PAGE TITLE			
LVDS CONNECTOR			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=VEMURI K901		SYNC DATE=06/25/2010	
PAGE TITLE			
LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	SIZE
			D
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SMIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	DMI_S2N	DCIE 85D	DCIE	DMI S2N P<3:0>	9 17
	DMI_S2N	DCIE 85D	DCIE	DMI S2N N<3:0>	9 17
	DMI_N2S	DCIE 85D	DCIE	DMI N2S P<3:0>	9 17
	DMI_N2S	DCIE 85D	DCIE	DMI N2S N<3:0>	9 17
	FDI_DATA	DCIE 85D	DCIE	FDI DATA P<7:0>	9 17
	FDI_DATA	DCIE 85D	DCIE	FDI DATA N<7:0>	9 17
		CHU 50S	CHU AGTT	FDI FSYNC<1..0>	9 17
		CHU 50S	CHU AGTT	FDI LSYNC<1..0>	9 17
		CHU 50S	CHU AGTT	FDI INT	9 17
	CPU_PECI	CHU 50S	DCIE	CPU PECI	10 19 45
	PM_SYNC	CHU 50S	CHU AGTT	PM SYNC	10 17
	PM_MEM_PWRGD	CHU 50S	CHU AGTT	PM MEM PWRGD	10 17 30
		CHU 50S	CHU ITP	XDP DBRESET L	10 23 26
		CHU 50S	CHU ITP	XDP CPU PRDY L	10 23
		CHU 50S	CHU ITP	XDP CPU PREQ L	10 23
		CHU 50S	CHU AGTT	PM EXT TS L<0>	
		CHU 50S	CHU AGTT	PM EXT TS L<1>	
	CPU_SM_RCOMP	CHU 27R4S	CHU COMP	CPU SM RCOMP<0>	10
	CPU_SM_RCOMP	CHU 27R4S	CHU COMP	CPU SM RCOMP<1>	10
	CPU_SM_RCOMP	CHU 27R4S	CHU COMP	CPU SM RCOMP<2>	10
		CHU 50S	CHU ITP	CPU CFG<11..0>	9 93
	CPU_CATERR_L	CHU 50S	CHU AGTT	CPU CATERR_L	10
		CHU 50S	CHU AGTT	CPU VCCIO_SEL	12
	CPU_PROCHOT_I	CHU 50S	CHU AGTT	CPU PROCHOT_L	10 46 68
	CPU_PWRGD	CHU 50S	CHU AGTT	CPU PWRGD	10 19 23
	PM_THRMTRIP_I	CHU 50S	CHU BMTI	PM THRMTRIP_L	10 19
	DMI_CLK100M	CLK DCIE 90D	CLK DCIE	DMI CLK100M CPU_P	10 16
	DMI_CLK100M	CLK DCIE 90D	CLK DCIE	DMI CLK100M CPU_N	10 16
	ITPCPU_CLK100M	CLK DCIE 90D	CLK DCIE	ITPCPU CLK100M_P	10 16
	ITPCPU_CLK100M	CLK DCIE 90D	CLK DCIE	ITPCPU CLK100M_N	10 16
	ITPXDP_CLK100M	CLK DCIE 90D	CLK DCIE	ITPXDP CLK100M_P	16 23
	ITPXDP_CLK100M	CLK DCIE 90D	CLK DCIE	ITPXDP CLK100M_N	16 23
	ITPCPU_CLK100M	CLK DCIE 90D	CLK DCIE	XDP CPU CLK100M_P	23
	ITPCPU_CLK100M	CLK DCIE 90D	CLK DCIE	XDP CPU CLK100M_N	23
		CPU 27R4S	CPU COMP	RDP COMP	9
		CPU 27R4S	CPU COMP	CPU PEG COMP	9
	XDP_TDI	CHU 50S	CHU ITP	XDP CPU TDI	10 23
	XDP_TDO	CHU 50S	CHU ITP	XDP CPU TDO	10 23
	XDP_TMS	CHU 50S	CHU ITP	XDP CPU TMS	10 23
	XDP_TCK	CHU 50S	CHU ITP	XDP CPU TCK	10 23
	XDP_TRST_I	CHU 50S	CHU ITP	XDP CPU TRST_L	10 23
	XDP_BPM_I	CHU 50S	CHU ITP	XDP BPM L<3..0>	10 23
	XDP_BPM_R_L	CHU 50S	CHU ITP	CPU CFG<15..12>	9 23
	(FSB_CPURST_L)	CHU 50S	CHU ITP	XDP CPURST_L	23
	CHU_VCCXG_SENSE	CHU 27R4S	CHU VCCSENSE	CPU VCCSENSE_P	12 68
	CHU_VCCXG_SENSE	CHU 27R4S	CHU VCCSENSE	CPU VCCSENSE_N	12 68
	CPU_VCCSENSE	CHU 27R4S	CHU VCCSENSE	CPU VCCIOSENSE_P	12 70
	CPU_VCCSENSE	CHU 27R4S	CHU VCCSENSE	CPU VCCIOSENSE_N	12 70
	CPU_VCCXG_SENSE	CHU 27R4S	CHU VCCSENSE	CPU AXG_SENSE_P	12 68
	CPU_VCCXG_SENSE	CHU 27R4S	CHU VCCSENSE	CPU AXG_SENSE_N	12 68
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU VDDO_SENSE_P	12
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU VDDO_SENSE_N	12
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU AXG_VALSENSE_P	9
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU AXG_VALSENSE_N	9
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU VCC_VALSENSE_P	9
	CHU_VALSENSE	CHU 27R4S	CHU VCCSENSE	CPU VCC_VALSENSE_N	9

```
CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>
```

SYNC MASTER=ANNE KROI		SYNC DATE=06/08/2010	
PAGE TITLE			
CPU Constraints			
 Apple Inc.		DRAWING NUMBER SIZE D	
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Memory Bus Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
Memory Net Properties							
ELECTRICAL_CONSTRAINT_SET		NET_TYPE					
		PHYSICAL	SPACING				
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK P<5..0>	11	27		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK N<5..0>	11	27		
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11	27		
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11	27		
MEM_A_CMT	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11	27		
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11	27		
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11	27		
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11	27		
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11	27		
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11	27		
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11	28		
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11	28		
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11	28		
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11	28		
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11	27	28	
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11	28		
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11	28		
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11	28		
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS P<0>	11	27	28	
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS N<0>	11	27	28	
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS P<1>	11	28		
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS N<1>	11	28		
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS P<2>	11	28		
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS N<2>	11	28		
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS P<3>	11	28		
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS N<3>	11	28		
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS P<4>	11	28		
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS N<4>	11	28		
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS P<5>	11	28		
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS N<5>	11	28		
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS P<6>	11	28		
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS N<6>	11	28		
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS P<7>	11	28		
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS N<7>	11	28		
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK P<5..0>	11	29		
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK N<5..0>	11	29		
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11	29		
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11	29		
MEM_B_CMT	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11	29		
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11	29		
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11	29		
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11	29		
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11	29		
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11	29		
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11	28		
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11	28		
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11	28		
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11	28		
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11	28	29	
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11	28		
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11	28		
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11	28		
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS P<0>	11	28	29	
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS N<0>	11	28	29	
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS P<1>	11	28		
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS N<1>	11	28		
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS P<2>	11	28		
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS N<2>	11	28		
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS P<3>	11	28		
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS N<3>	11	28		
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS P<4>	11	28		
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS N<4>	11	28		
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS P<5>	11	28		
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS N<5>	11	28		
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS P<6>	11	28		
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS N<6>	11	28		
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS P<7>	11	28		
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS N<7>	11	28		
Memory Bus Spacing Group Assignments							
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM	MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM	MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM	MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM	MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM	MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM	MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL	MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM	MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM	MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM	MEM_DATA	MEM_DQS	*	MEM_DATA2MEM
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM	MEM_CLK	*	*	MEM_2OTHER
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM	MEM_CTRL	*	*	MEM_2OTHER
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM	MEM_CMD	*	*	MEM_2OTHER
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM	MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM	MEM_DQS	*	*	MEM_2OTHER
Need to support MEM*-style wildcards!							
DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).							
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.							
DQ to DQS matching per byte lane should be within 0.127mm.							
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].							
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.							
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.							
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.							
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.							
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.							
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5							
8	7	6	5	4	3	2	1

D

C

B

A

D

C

B

A

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P
DP_85D	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SCL
DP_85D	T29_I2C_55S	T29_I2C	I2C T29_SDA
DP_85D	T29_I2C_55S	T29_I2C	
DP_85D	T29_SPI_55S	T29_SPI	T29_SPI_CLK
DP_85D	T29_SPI_55S	T29_SPI	T29_SPI_MOSI
DP_85D	T29_SPI_55S	T29_SPI	T29_SPI_MISO
DP_85D	T29_SPI_55S	T29_SPI	T29_SPI_CS_L
DP_85D	T29_SPI_55S	T29_SPI	
DP_85D	T29DP_80D	T29DP	T29_R2D C P<3..0>
DP_85D	T29DP_80D	T29DP	T29_R2D C N<3..0>
DP_85D	T29DP_100D	T29DP	T29_D2R P<3..0>
DP_85D	T29DP_100D	T29DP	T29_D2R N<3..0>

Only used on hosts supporting T29 video-in

T29/DP Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DP_85D	T29DP_80D	T29DP	T29_R2D P<0>
DP_85D	T29DP_80D	T29DP	T29_R2D N<0>
DP_85D	T29DP_80D	T29DP	T29_R2D P<1>
DP_85D	T29DP_80D	T29DP	T29_R2D N<1>
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<1..0>
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<1..0>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<0>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<0>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<1>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<1>
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P
DP_85D	T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P
DP_85D	T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N
DP_85D	T29DP_80D	T29DP	T29DPA_ML_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPA_ML_N<3..0>
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N
DP_85D	T29DP_80D	T29DP	T29_R2D P<2>
DP_85D	T29DP_80D	T29DP	T29_R2D N<2>
DP_85D	T29DP_80D	T29DP	T29_R2D P<3>
DP_85D	T29DP_80D	T29DP	T29_R2D N<3>
DP_85D	T29DP_80D	T29DP	T29_R2D C F P<3..2>
DP_85D	T29DP_80D	T29DP	T29_R2D C F N<3..2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<2>
DP_85D	T29DP_100D	T29DP	T29_D2R C P<3>
DP_85D	T29DP_100D	T29DP	T29_D2R C N<3>
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P
DP_85D	T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P
DP_85D	T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N
DP_85D	T29DP_80D	T29DP	T29DPB_ML_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_N<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>
DP_85D	T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_P
DP_85D	T29DP_80D	T29DP	DP_B_EXT_AUXCH_N

Only used on dual-port hosts.

SYNC MASTER=Master

SYNC DATE=06/21/2010

T29 Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1701_550	*	+1/1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1/1_DIFFPAIR	+1/1_DIFFPAIR
THERM_1701_550	*	+1/1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1/1_DIFFPAIR	+1/1_DIFFPAIR
DIFFPAIR	*	+1/1_DIFFPAIR			+1/1_DIFFPAIR	+1/1_DIFFPAIR	+1/1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENHTRCOBH	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENRT_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	+	GND_P2046
PCIE	GND	+	GND_P2046
SATA	GND	+	GND_P2046
USB	GND	+	GND_P2046
CLK_PCIE	SB_POWER	+	PWR_P2046
SATA	SB_POWER	+	PWR_P2046
USB	SB_POWER	+	PWR_P2046

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLE	QND	*	QND_P2984
MEM_CND	QND	*	QND_P2984
MEM_CTLG	QND	*	QND_P2984
MEM_DATA	QND	*	QND_P2984
MEM_PQIS	QND	*	QND_P2984

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYC	SPACING	NET_TYPE	
	ENET_10G	ENETCONN	ENETCONN_P<3...0>	38
	ENET_10G	ENETCONN	ENETCONN_N<3...0>	38
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_ERVRV_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_ERVRV_OUT_N	42
	SATA_90D	SATA	SATA_HDD_R2D_ERVRV_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_ERVRV_IN_N	42
9391	SATA_90D	SATA	SATA_HDD_D2R_ERVRV_IN_P	42
9391	SATA_90D	SATA	SATA_HDD_D2R_ERVRV_IN_N	42
9391	SATA_90D	SATA	SATA_HDD_R2D_ERVRV_OUT_P	42
9391	SATA_90D	SATA	SATA_HDD_R2D_ERVRV_OUT_N	42
9391	THRM_1701_55C	THRM	CPUTHERMS_D2_P	51
9391	THRM_1701_55C	THRM	CPUTHERMS_D2_N	51
9391	THRM_1701_55C	THRM	CPU_THERMD_P	9 51
9391	THRM_1701_55C	THRM	CPU_THERMD_N	9 51
9391	THRM_1701_55C	THRM	T29_THERMD_P	34 51
9391	THRM_1701_55C	THRM	T29_THERMD_N	51
9391	THRM_1701_55C	THRM	T29THERMS_D2_P	51
9391	THRM_1701_55C	THRM	T29THERMS_D2_N	51
9391	THRM_1701_55C	THRM	ISNS_HS_COMPUTING_N	50
9391	THRM_1701_55C	THRM	ISNS_HS_COMPUTING_P	50
9391	THRM_1701_55C	THRM	ISNS_HS_OTHER_N	50
9391	THRM_1701_55C	THRM	ISNS_HS_OTHER_P	50
9391	THRM_1701_55C	THRM	CPUVCCIOS0_CS_N	49 70
9391	THRM_1701_55C	THRM	CPUVCCIOS0_CS_P	49 70
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS1_P	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS1_N	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS2_P	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS2_N	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISNSIG_P	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISNSIG_N	49 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISUM_R_P	49
9391	THRM_1701_55C	THRM	CPUIMVP_ISUM_R_N	49
9391	THRM_1701_55C	THRM	CPUIMVP_ISUMG_R_P	49
9391	THRM_1701_55C	THRM	CPUIMVP_ISUMG_R_N	49
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS_P	49
9391	THRM_1701_55C	THRM	CPUIMVP_ISNS_N	49
9391	THRM_1701_55C	THRM	VCCBARG_CS_P	65
9391	THRM_1701_55C	THRM	VCCBARG_CS_N	65
9391	THRM_1701_55C	THRM	CPUIMVP_ISUMG_P	61 61
9391	THRM_1701_55C	THRM	CPUIMVP_ISUMG_N	61 61
9391	THRM_1701_55C	THRM	ISNS_CPU_N	
9391	THRM_1701_55C	THRM	ISNS_CPU_P	
9391	THRM_1701_55C	THRM	ISNS_HDD_N	
9391	THRM_1701_55C	THRM	ISNS_HDD_P	
9391	THRM_1701_55C	THRM	ISNS_HDD_R_N	
9391	THRM_1701_55C	THRM	ISNS_HDD_R_P	
9391	THRM_1701_55C	THRM	ISNS_LCDCLKIT_N	
9391	THRM_1701_55C	THRM	ISNS_LCDCLKIT_P	
9391	THRM_1701_55C	THRM	ISNS_ODD_N	
9391	THRM_1701_55C	THRM	ISNS_ODD_P	
9391	THRM_1701_55C	THRM	ISNS_ODD_R_N	
9391	THRM_1701_55C	THRM	ISNS_ODD_R_P	
9391	THRM_1701_55C	THRM	ISNS_P1V8GPU_N	
9391	THRM_1701_55C	THRM	ISNS_P1V8GPU_P	
9391	THRM_1701_55C	THRM	ISNS_P1V8GPU_R_N	
9391	THRM_1701_55C	THRM	ISNS_P1V8GPU_R_P	
9391	LVDS_90D	LVDS	LVDS_CONN_A_CLK_P_N	6 74
9391	LVDS_90D	LVDS	LVDS_CONN_A_CLK_P_P	6 74


K90i Specific Net Properties

[illegible]

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	MD, TVFF, BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	-50_OHM_SE	-50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	-DEFAULT	-DEFAULT	10 MM	-DEFAULT	-DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHP_SR	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHP_SR	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SE	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SE	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SS	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SS	ISL10	N	0.145 MM	0.1 MM	<STANDARD	<STANDARD	<STANDARD
37_OHM_SS	ISL3, ISL4, ISL9	Y	0.145 MM	0.1 MM	<STANDARD	<STANDARD	<STANDARD
37_OHM_SS	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
2764_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
2764_OHM_SE	*	Y	0.235 MM	0.2 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_00M_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_00M_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
\$S_OBM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
\$S_OBM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
\$S_OBM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
\$S_OBM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM	0.200 MM		0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL9, ISL4	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM	0.250 MM	0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OBM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
80_OBM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OBM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OBM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	-DEFAULT	?
BGA_P1MM	*	-DEFAULT	?
BGA_P2MM	*	-DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P10M
MEM_CLK	*	BGA	BGA_P20M
CLK_PCE	*	BGA	BGA_P30M
CLK_SLOW	*	BGA	BGA_P20M

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2:5:1_SPACING	*	0.15 MM	?
2:1:1_SPACING	*	0.2 MM	?
2:5:1_SPACING	*	0.25 MM	?
3:1:1_SPACING	*	0.3 MM	?
4:1:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	* 1	Y	<STANDARD	<STANDARD	<STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_NGA	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF
100_DIFF_NGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_NGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers

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